PG411 A01

GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

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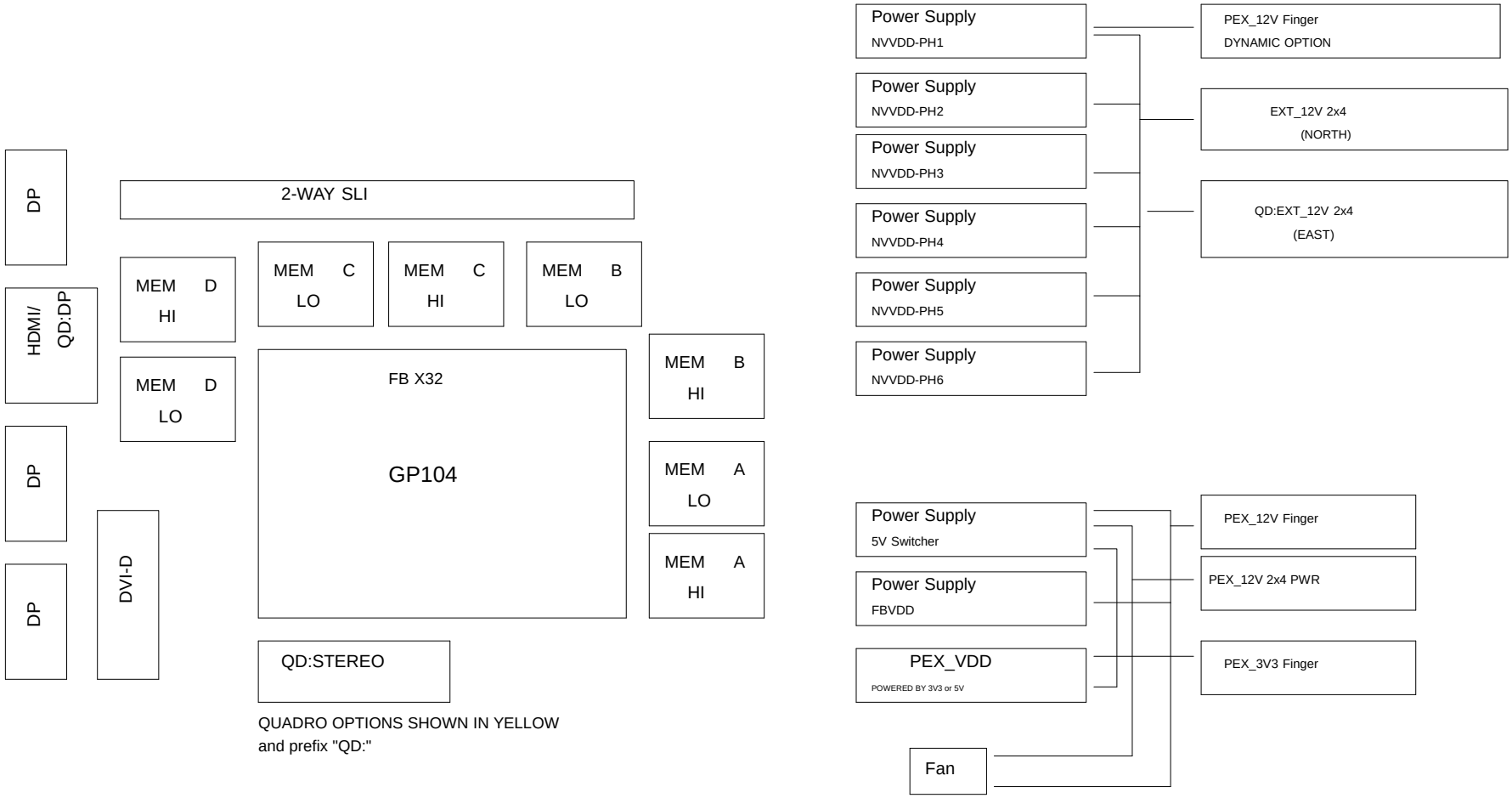
Page2: Block Diagram



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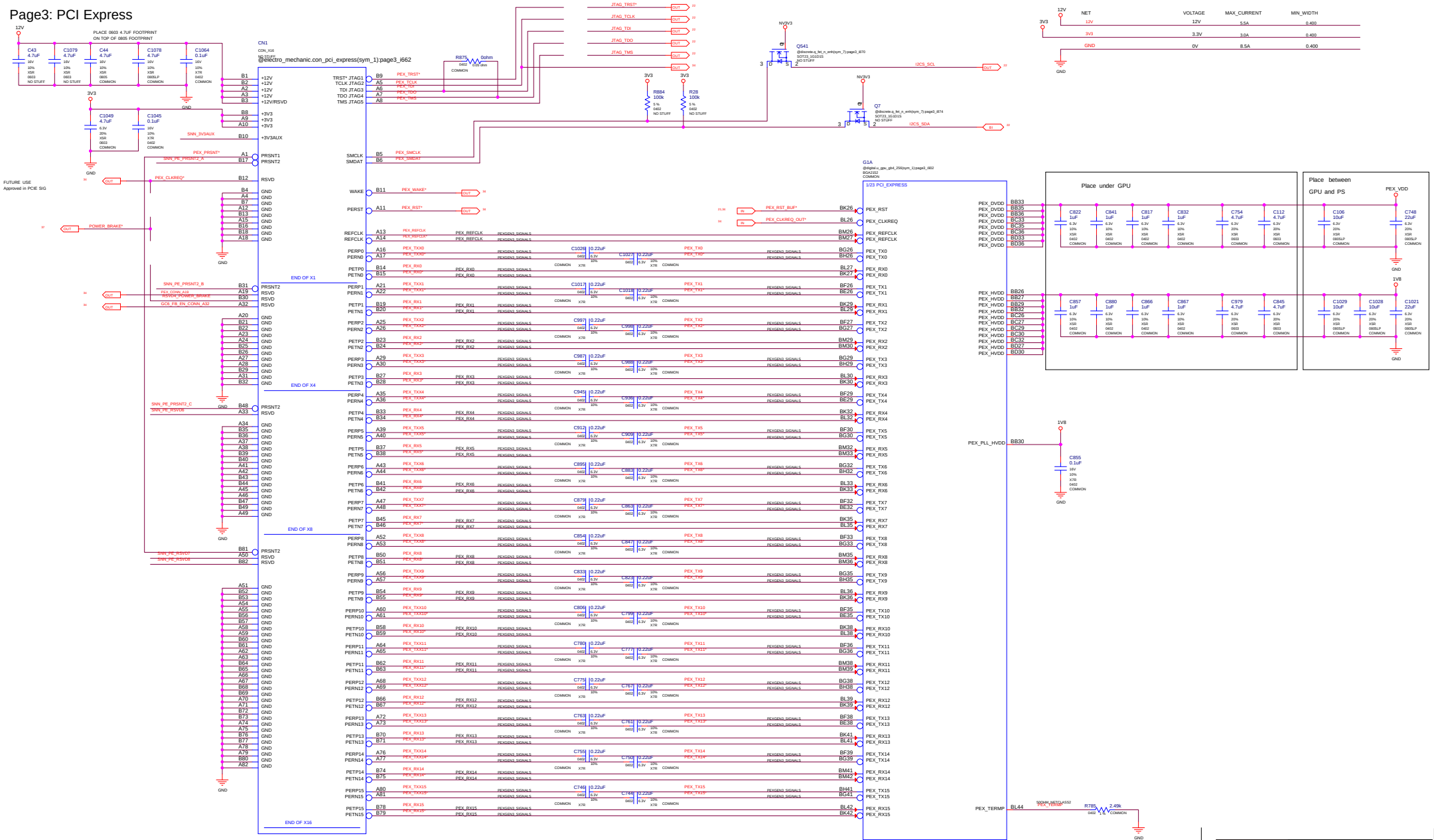
Page3: PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.400
3V3	3.3V	3.0A	0.400
GND	0V	8.5A	0.400

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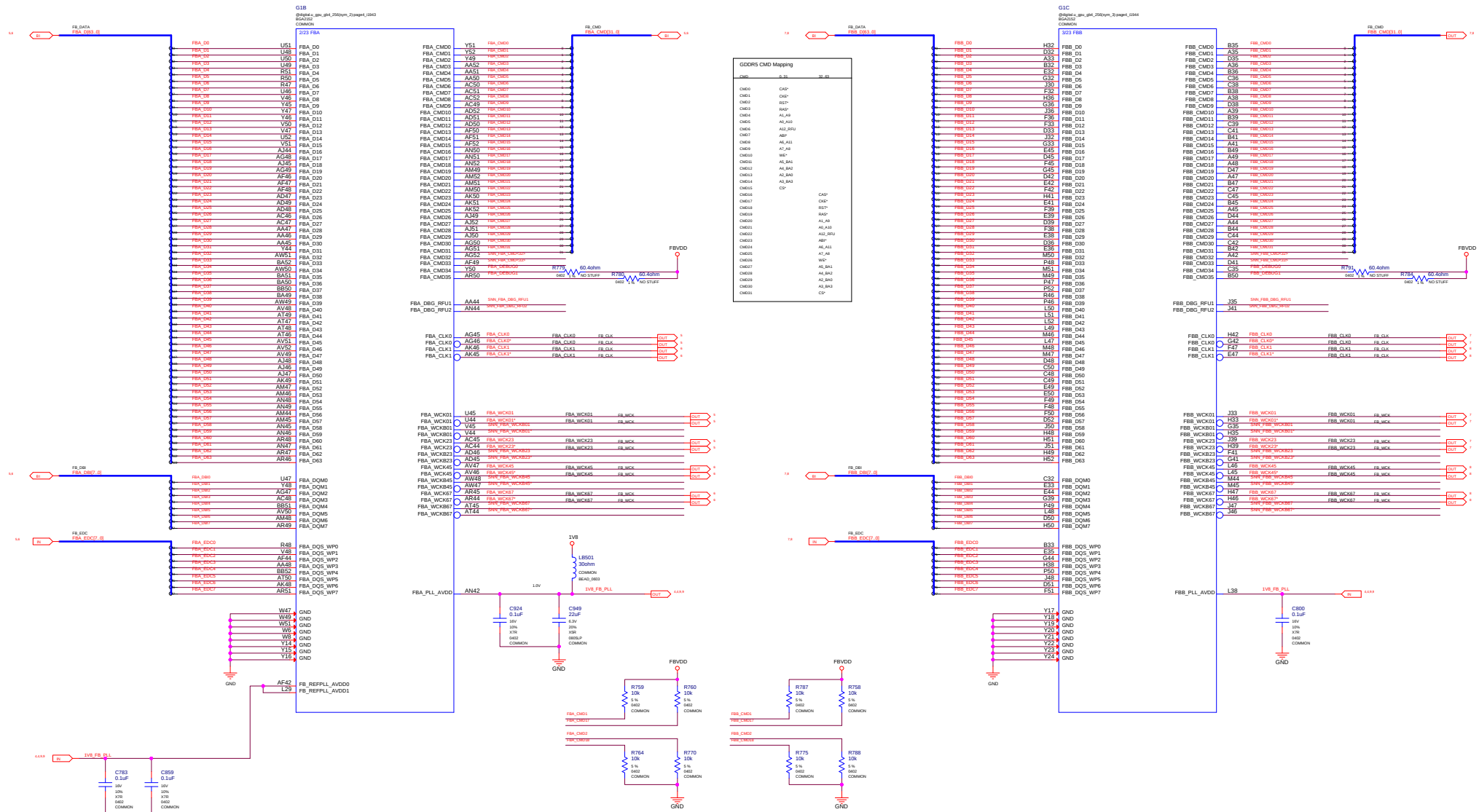
Page4: MEMORY: GPU Partition A/B



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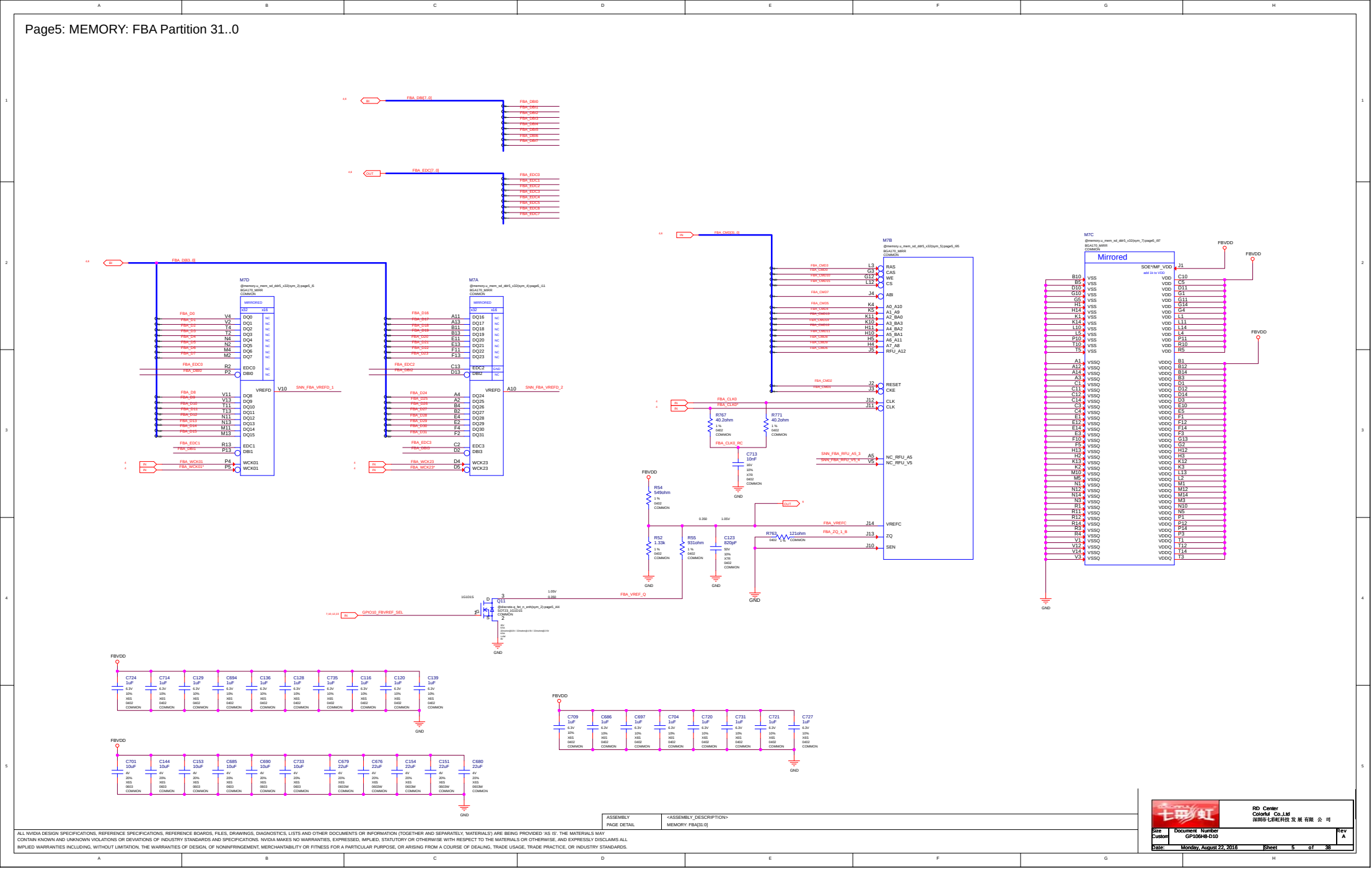
Page5: MEMORY: FBA Partition 31..0



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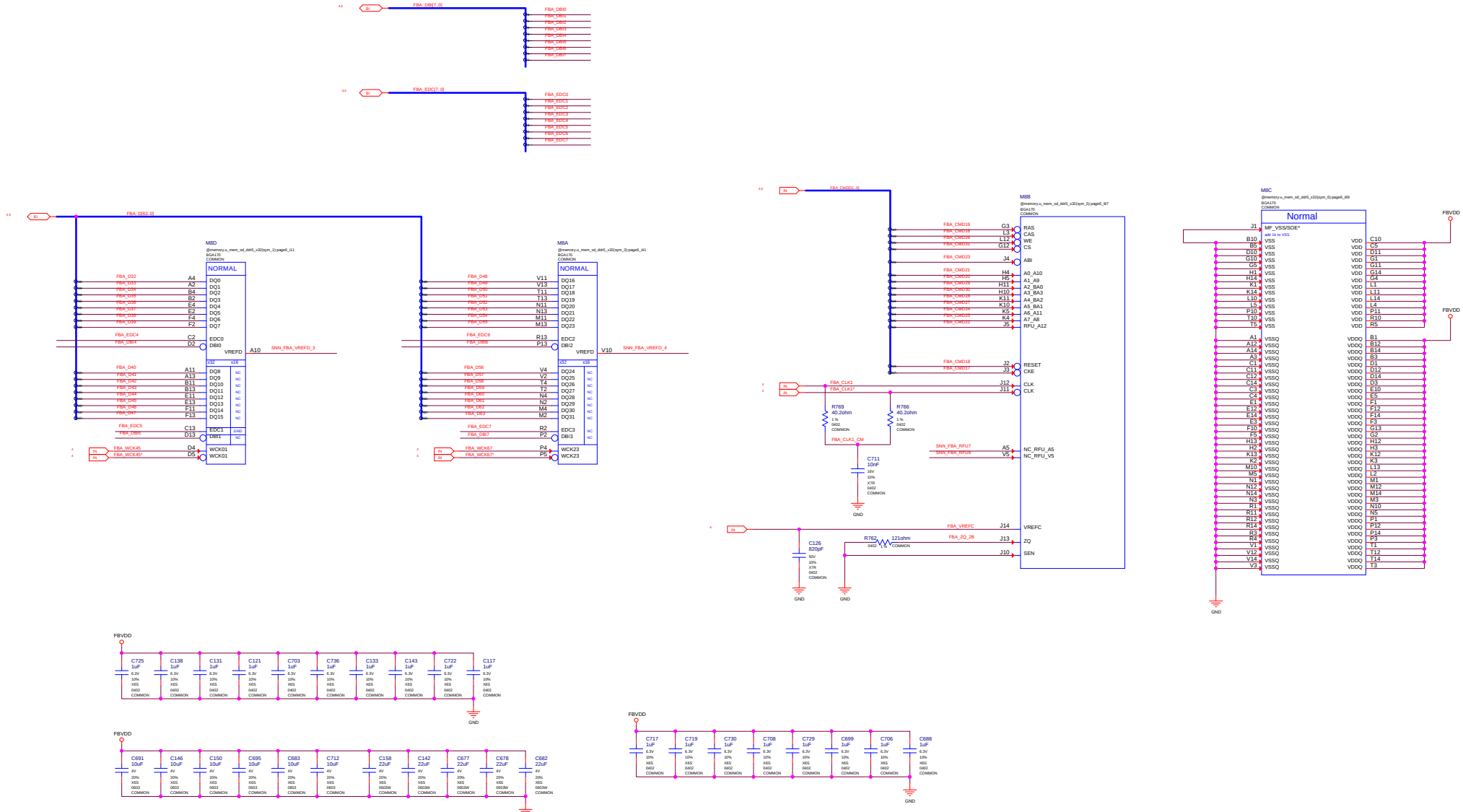
Page6: MEMORY: FBA Partition 63..32



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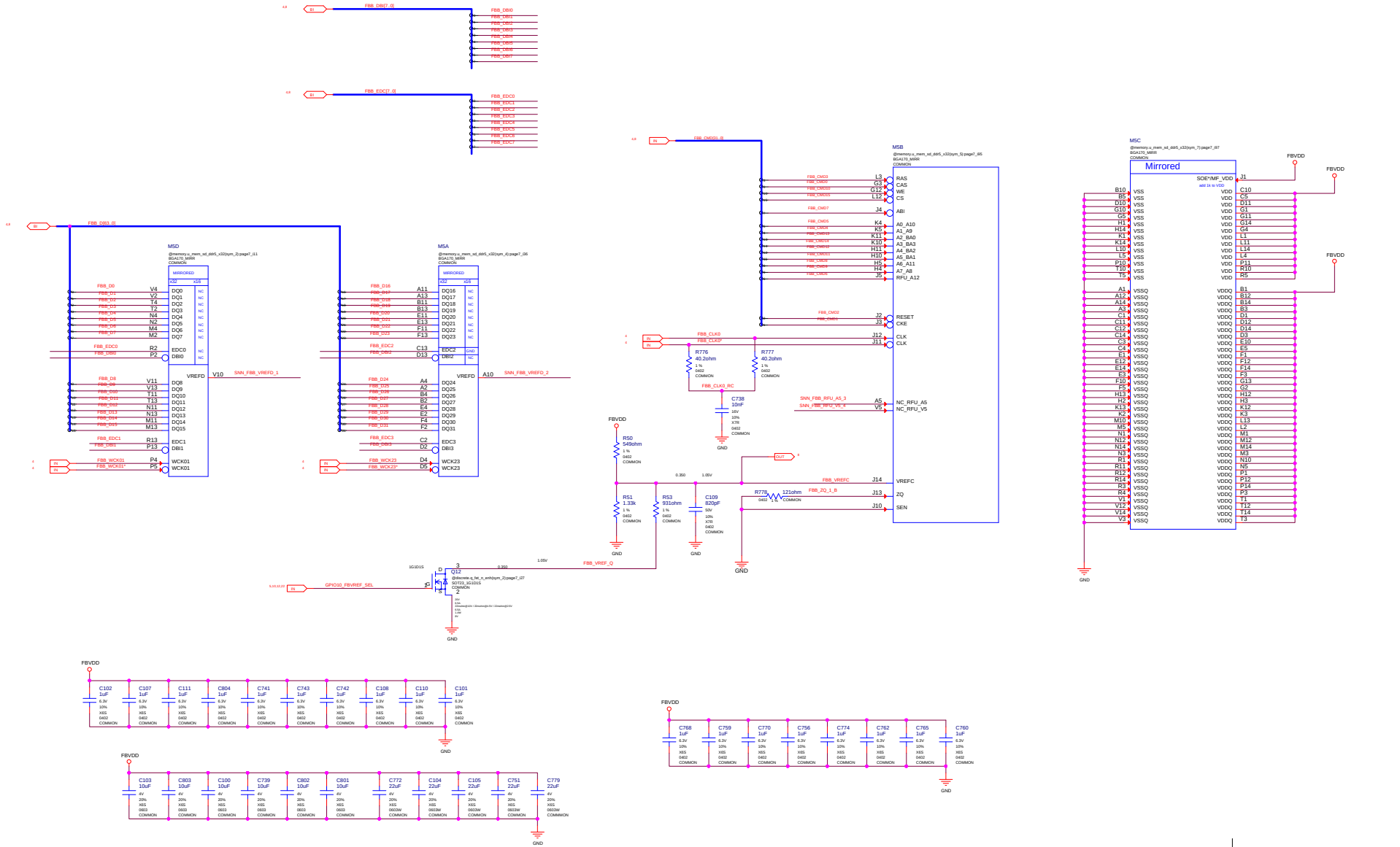

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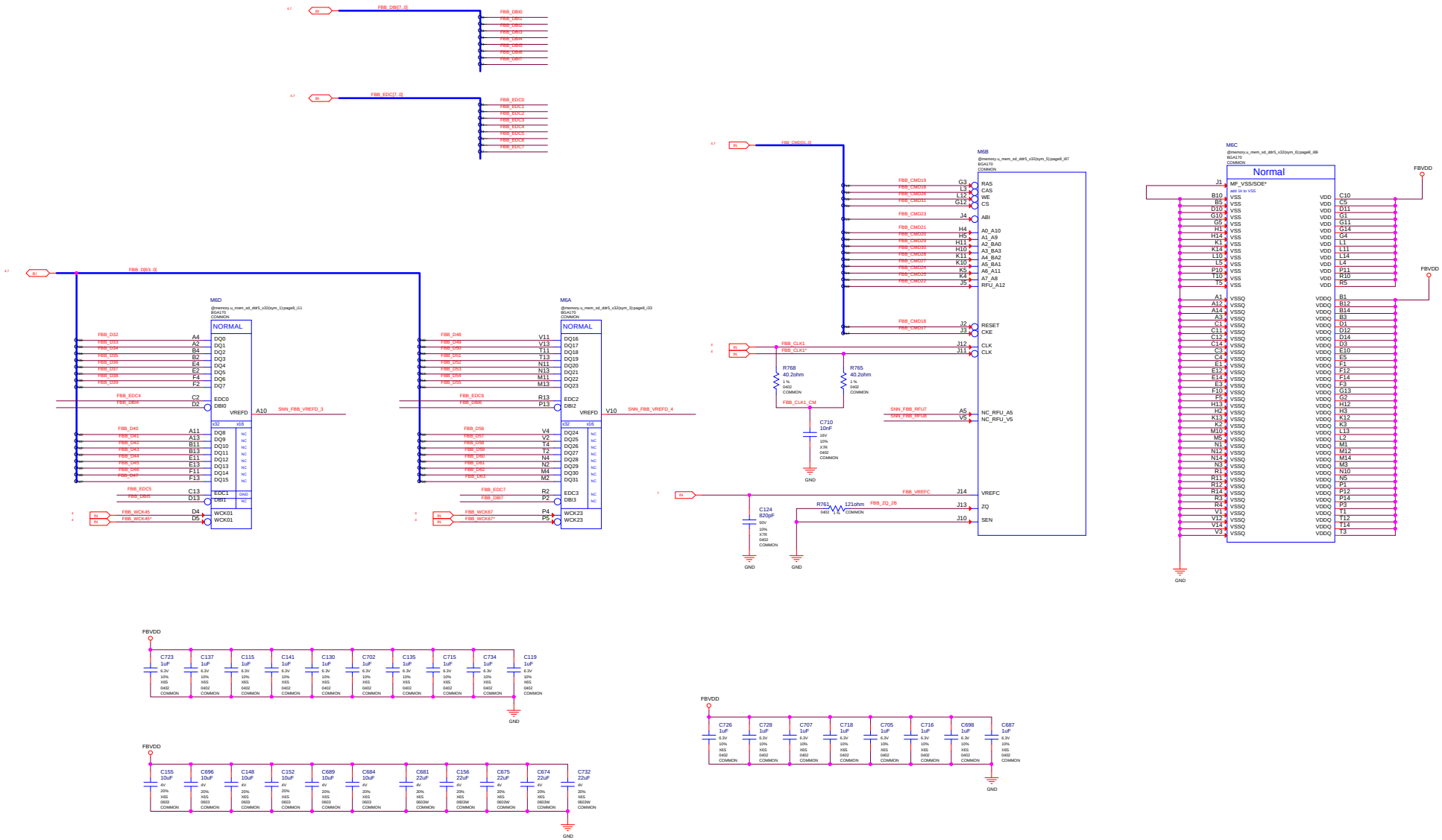

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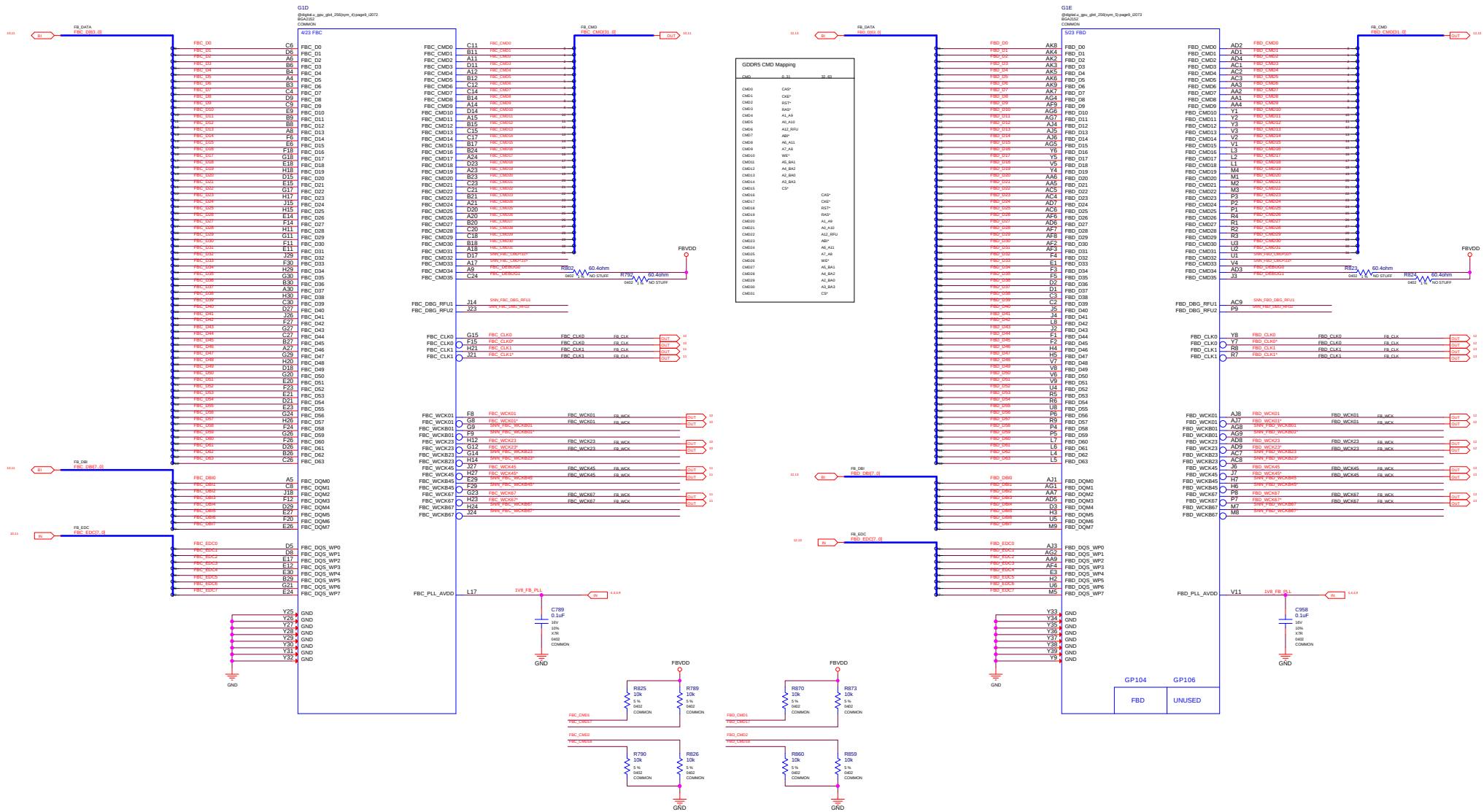

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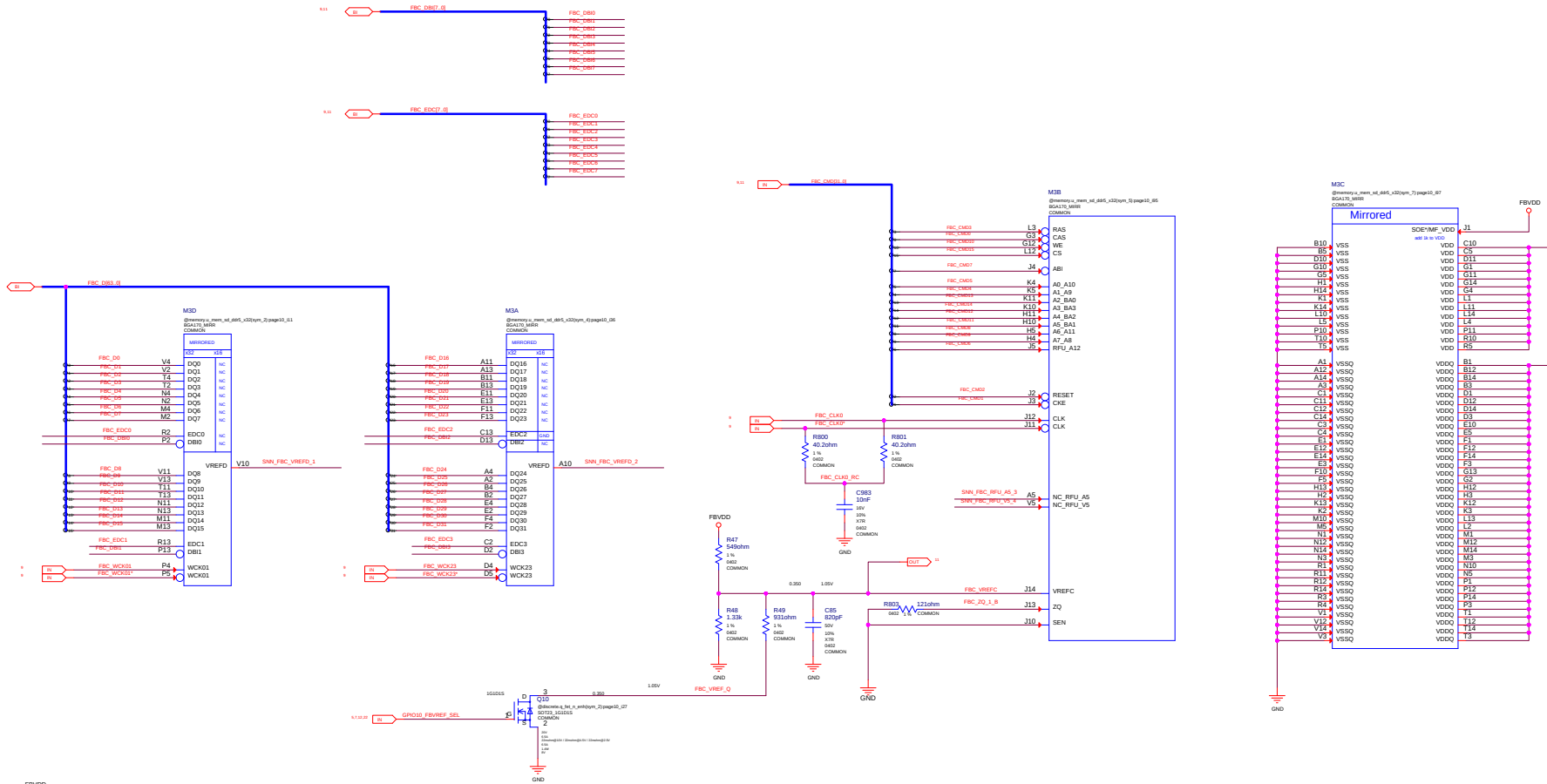
Page10: MEMORY: FBC Partition 31..0



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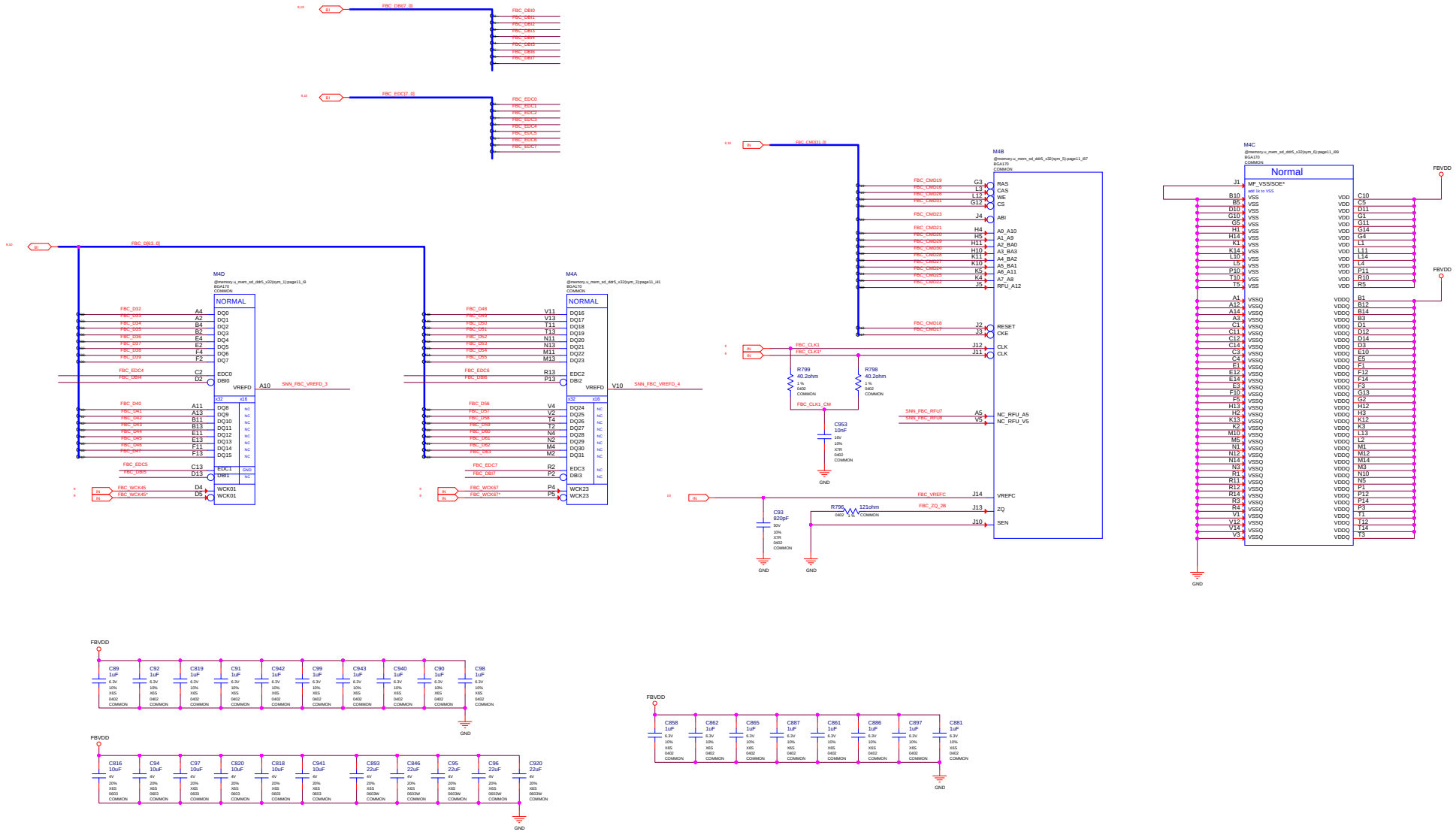

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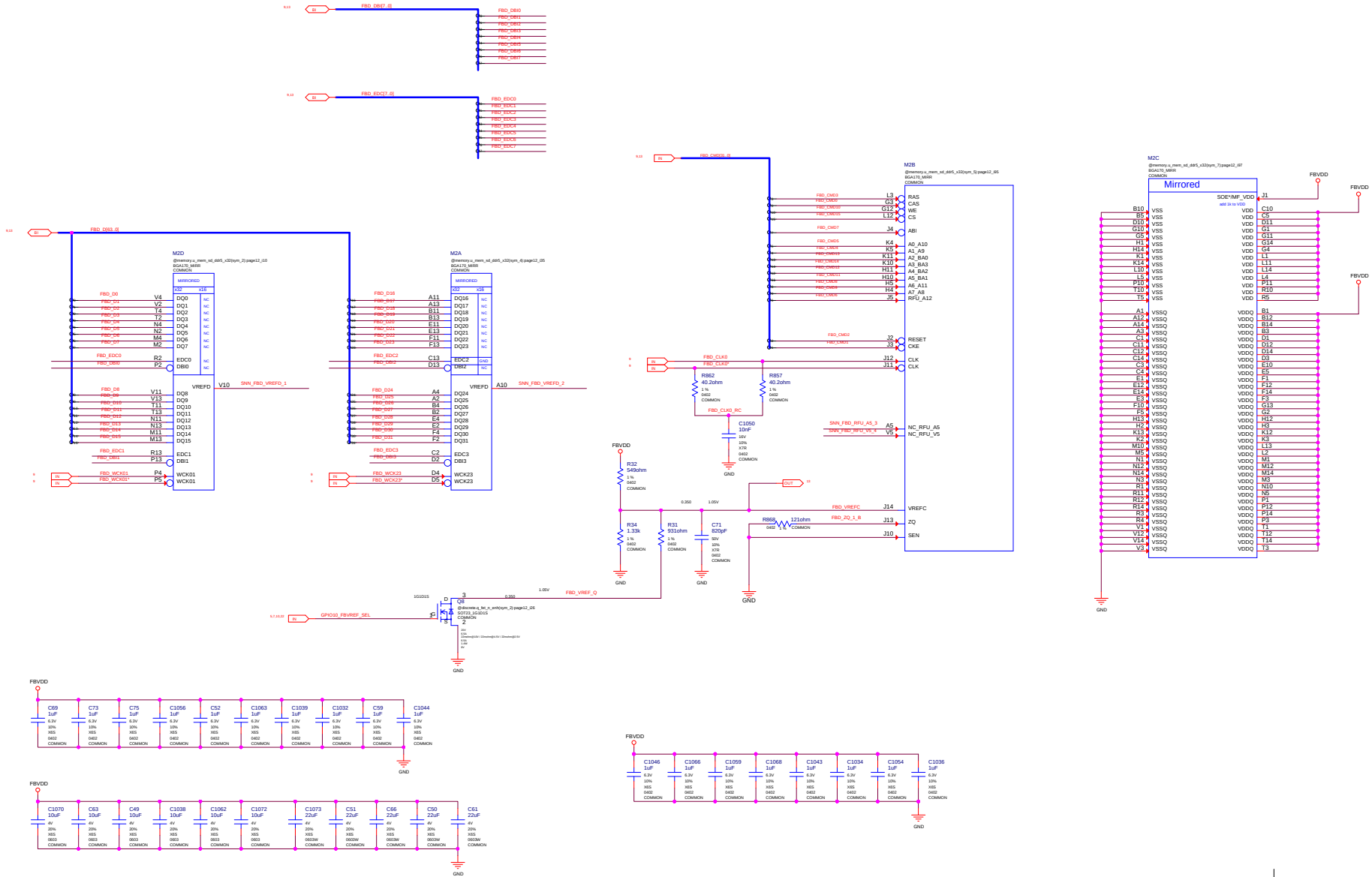

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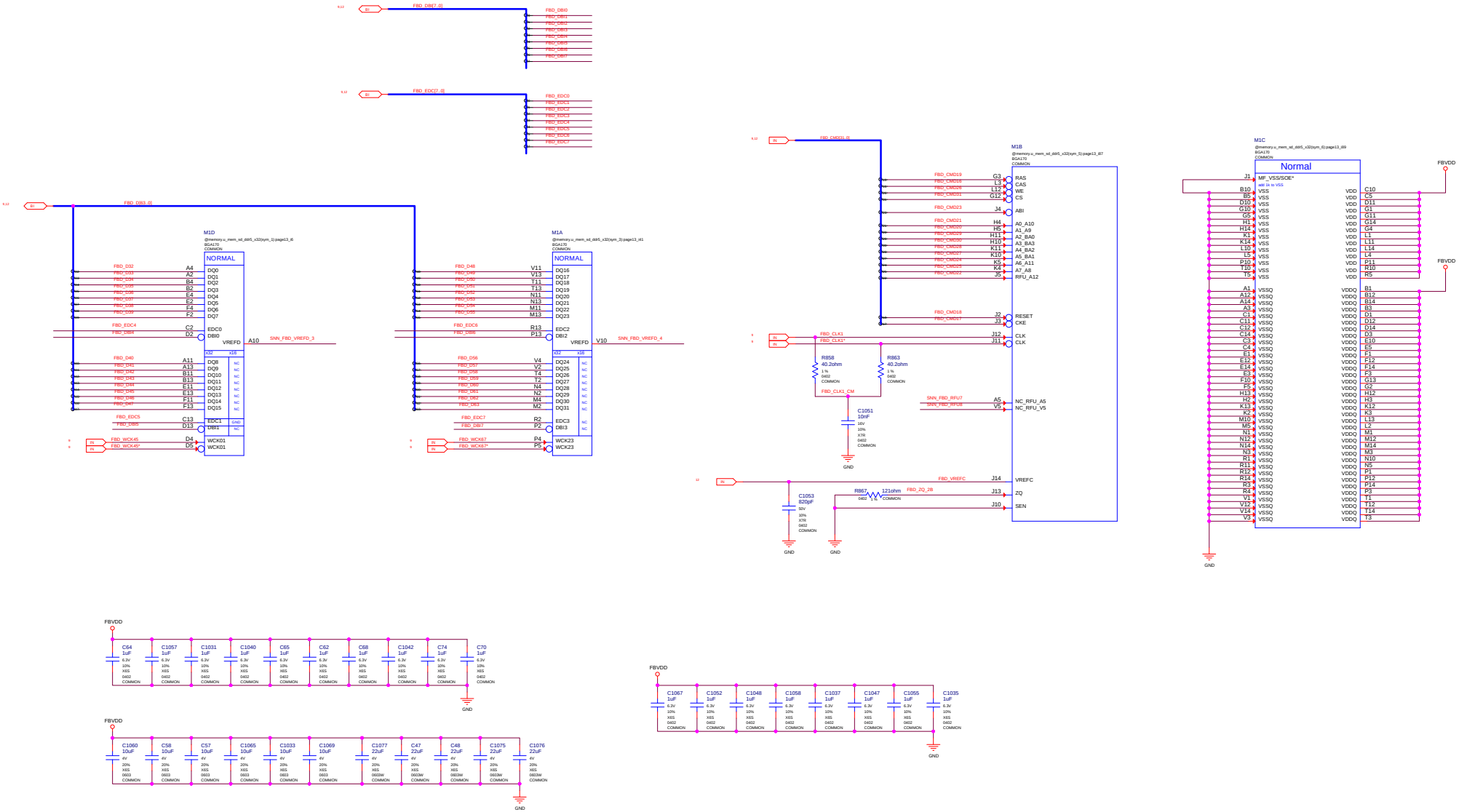

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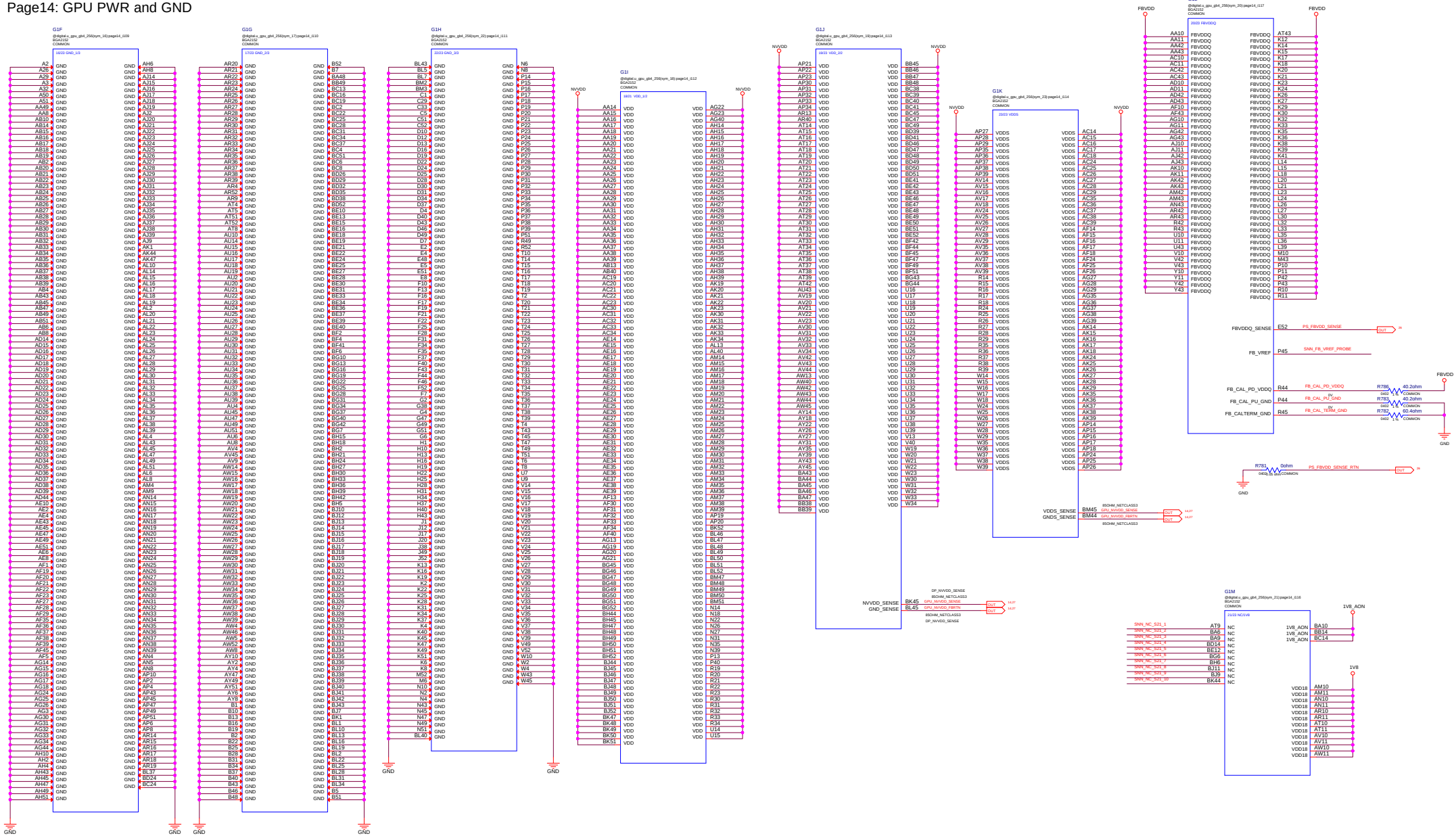
Page14: GPU PWR and GND



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PAGE DETAIL	GPU PWR and GND

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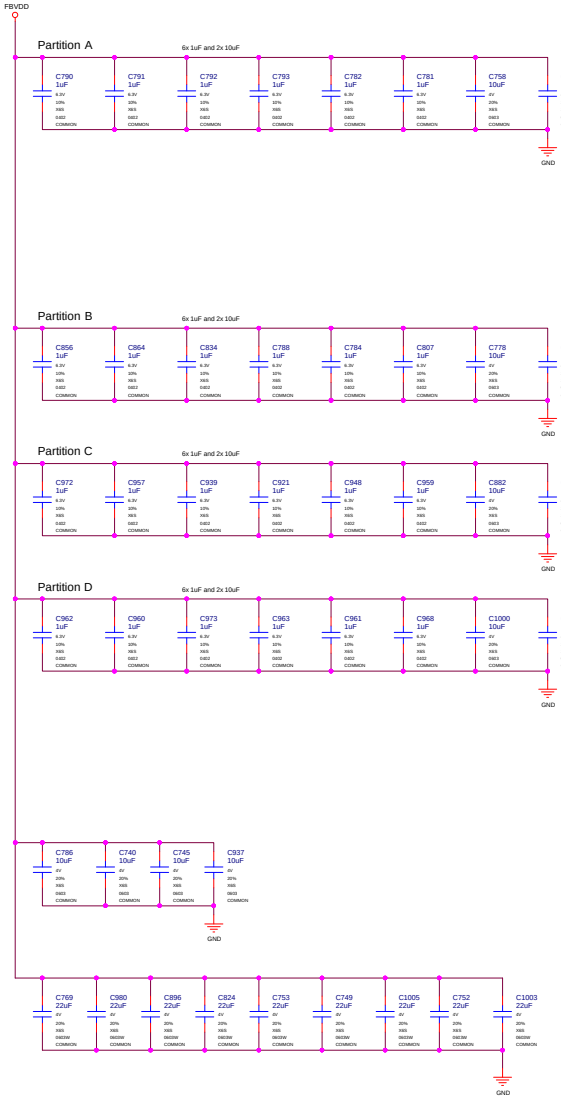
Page15: GPU Decoupling

FBVDD



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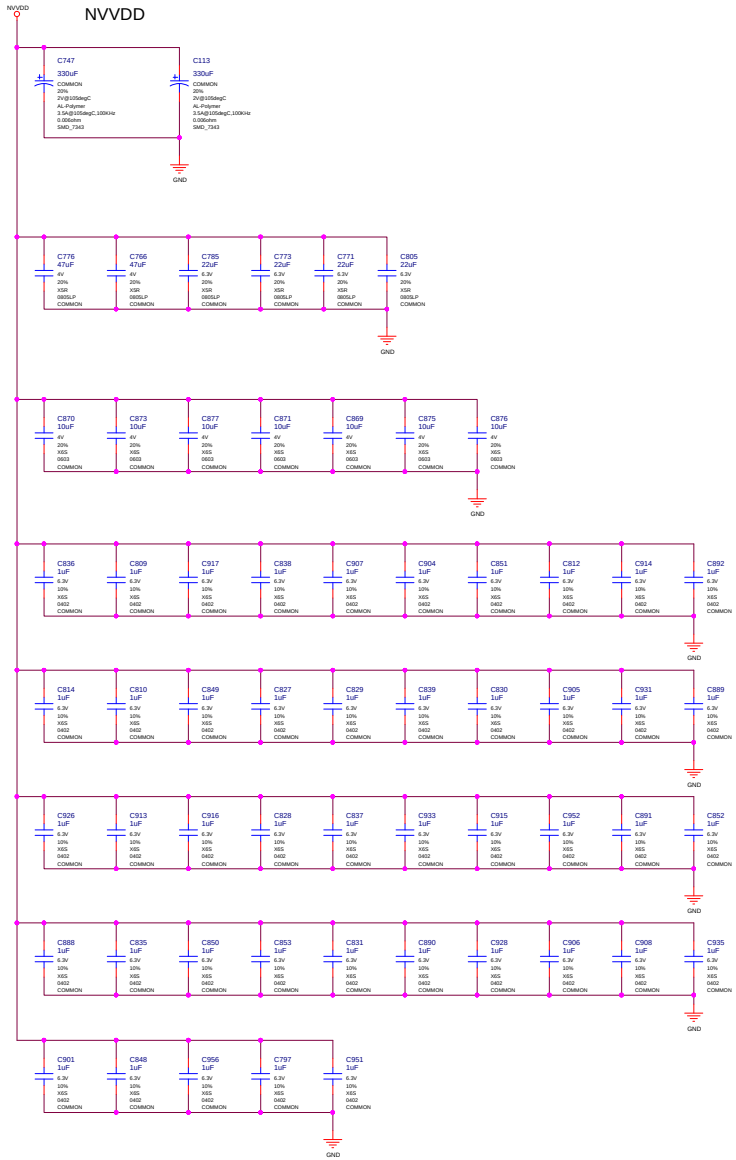

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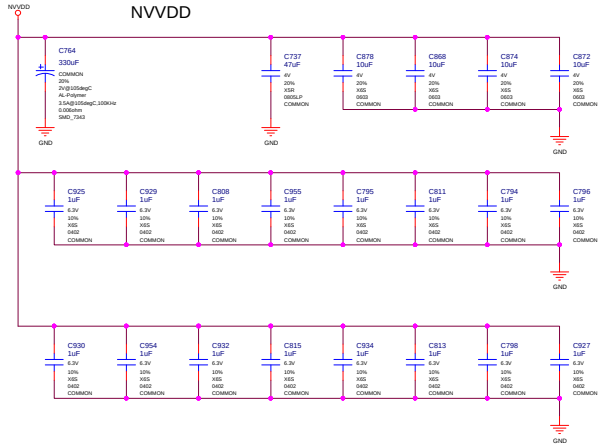

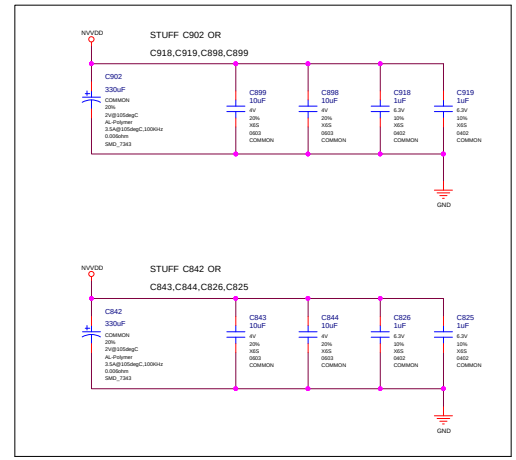

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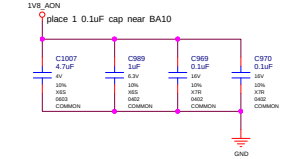
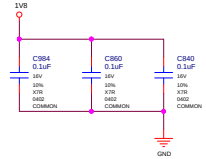


place 1 0.1uF cap for BB14 and BC14 to share

VDD18



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PAGE DETAIL	GPU Decoupling

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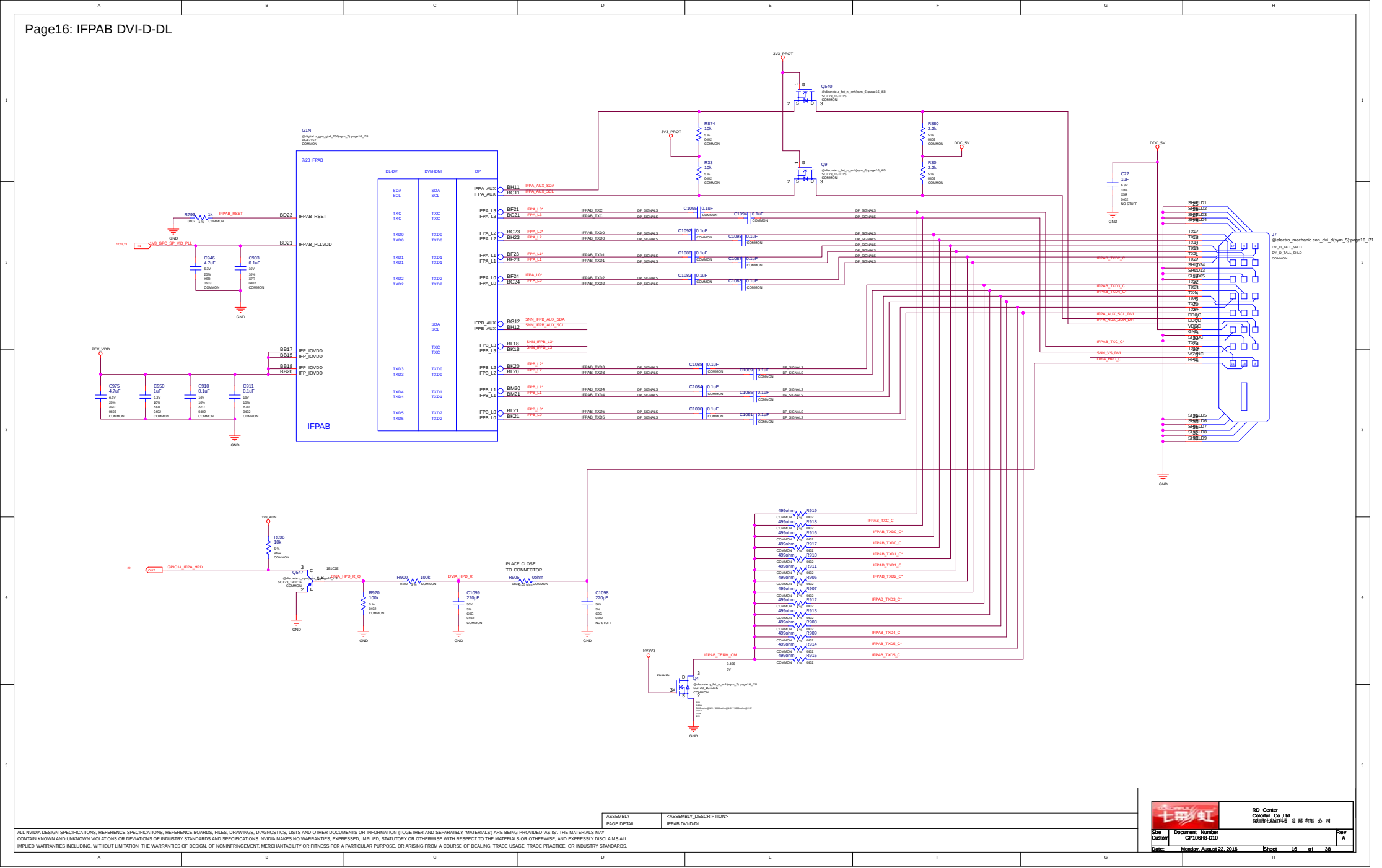
Page16: IFPAB DVI-D-DL



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPAB DVI-D-DL

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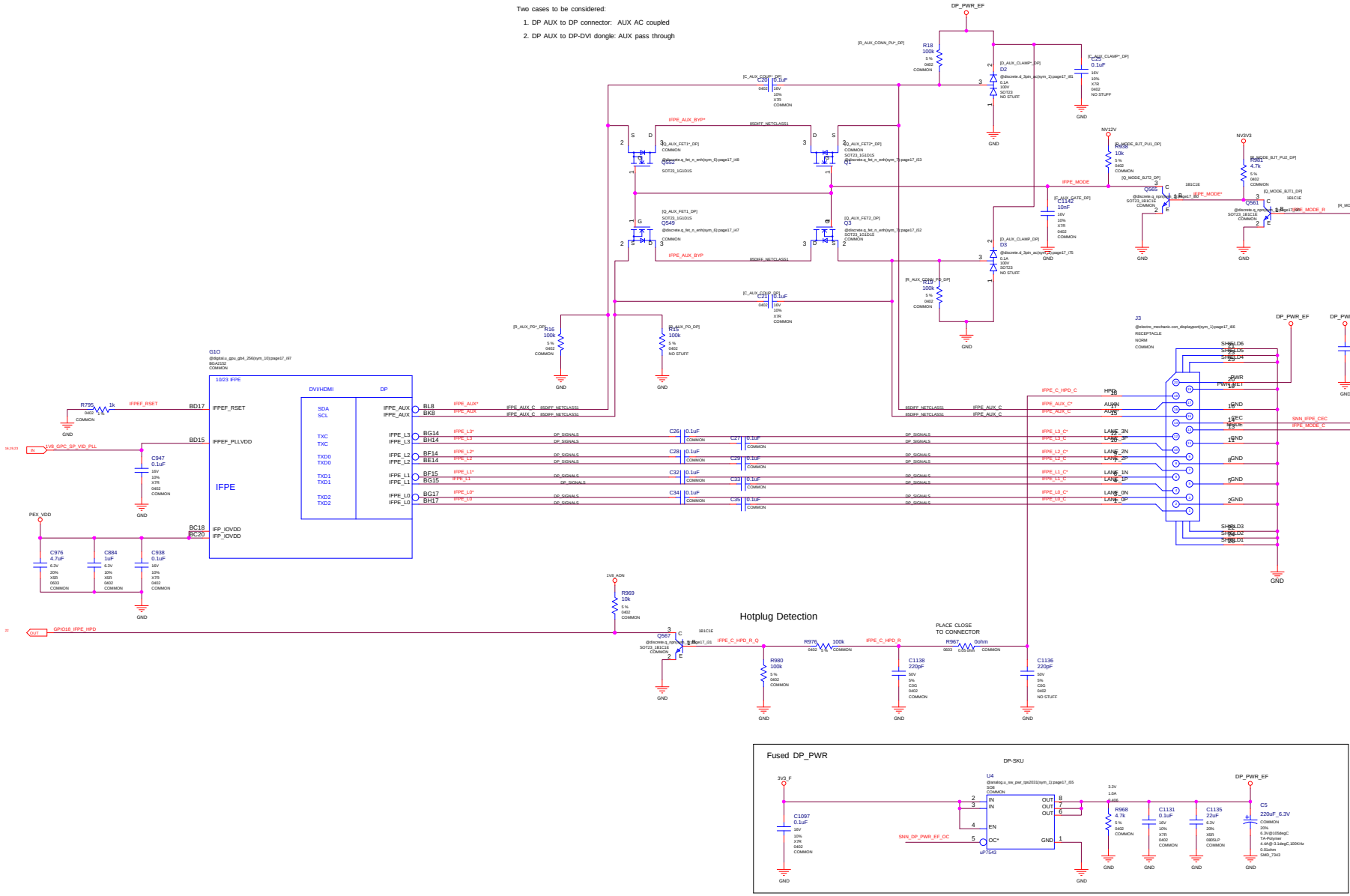
Page17: IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPE DP

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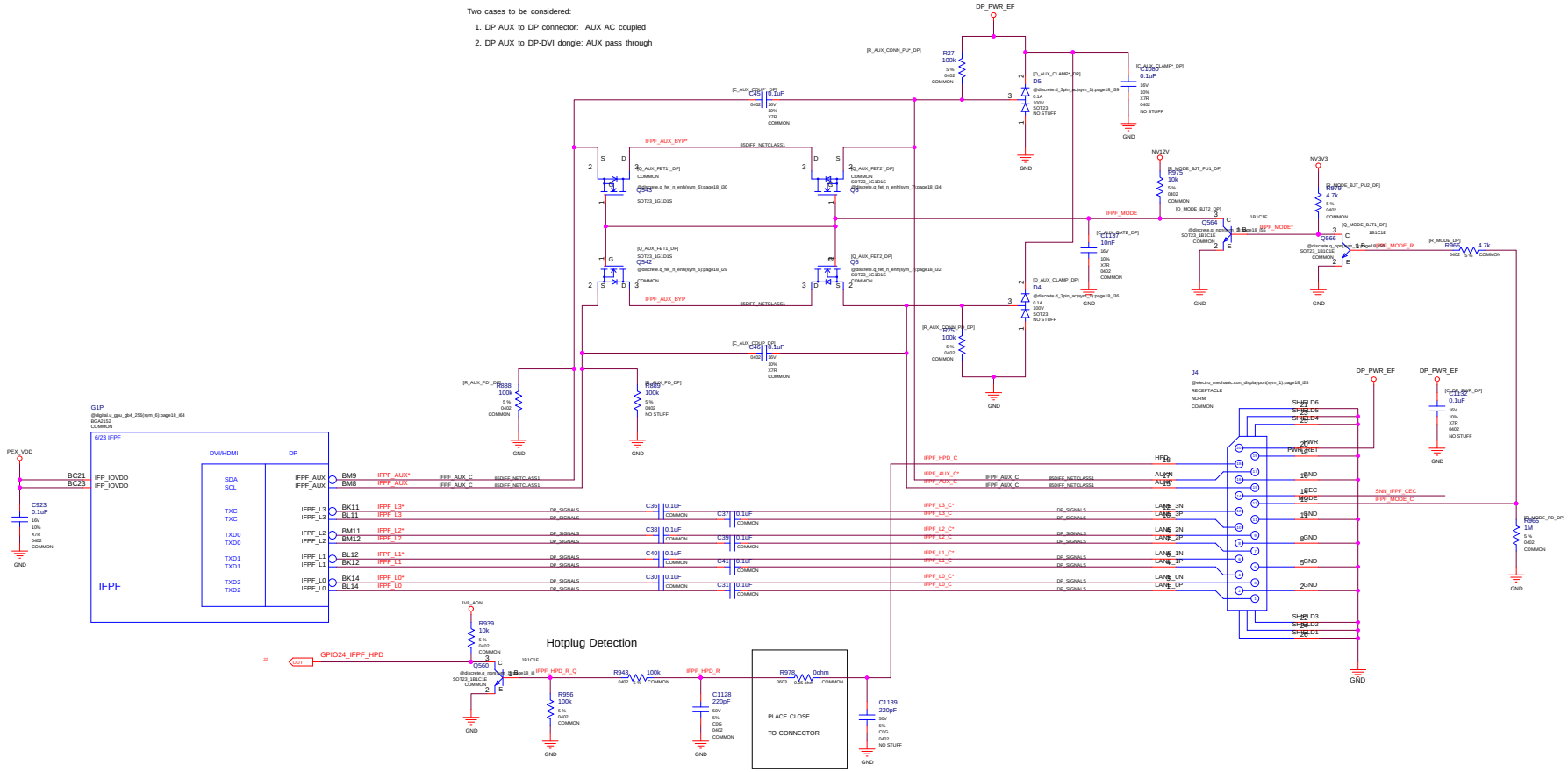
Page18: IFPF DP



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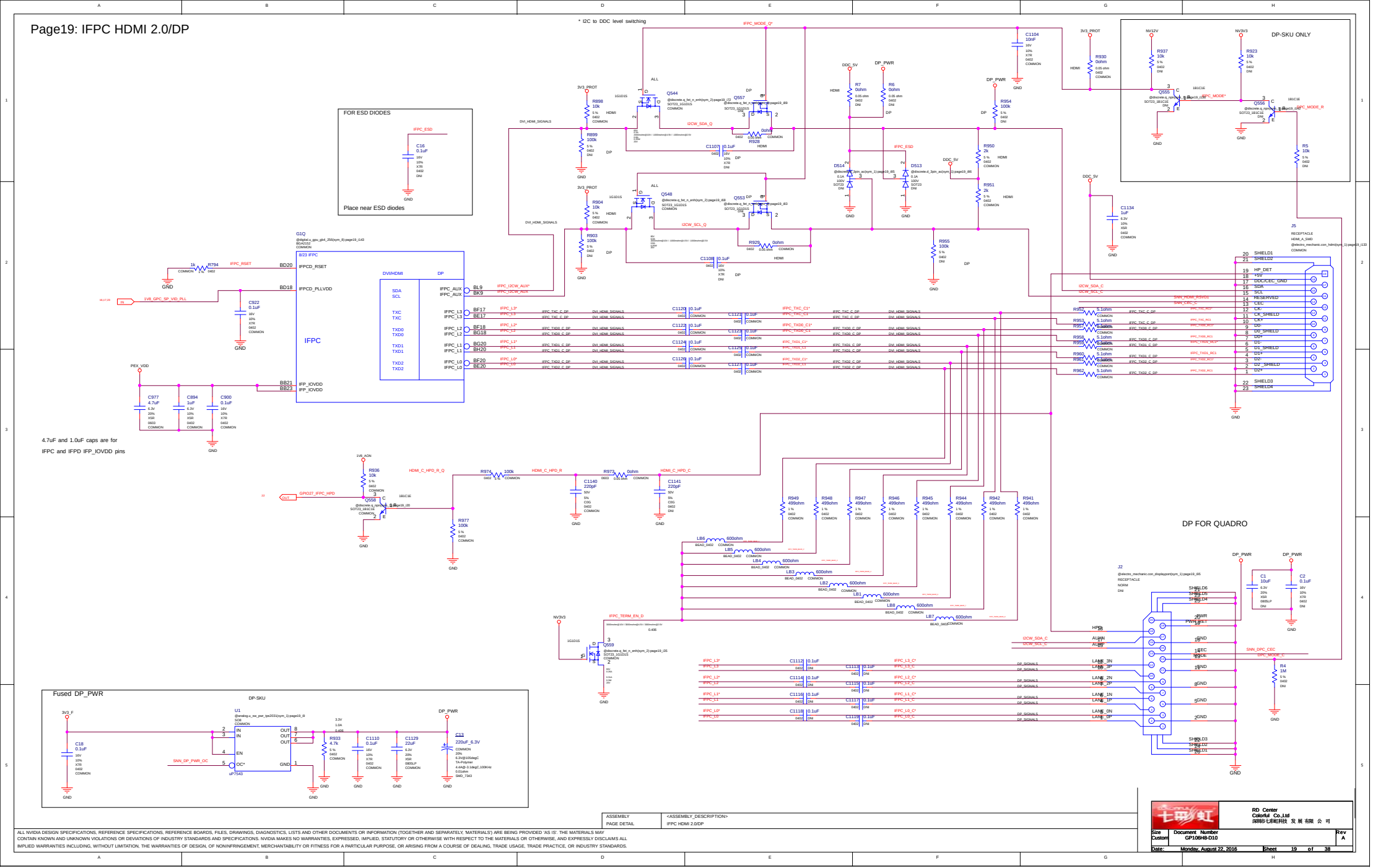
Page19: IFPC HDMI 2.0/DP



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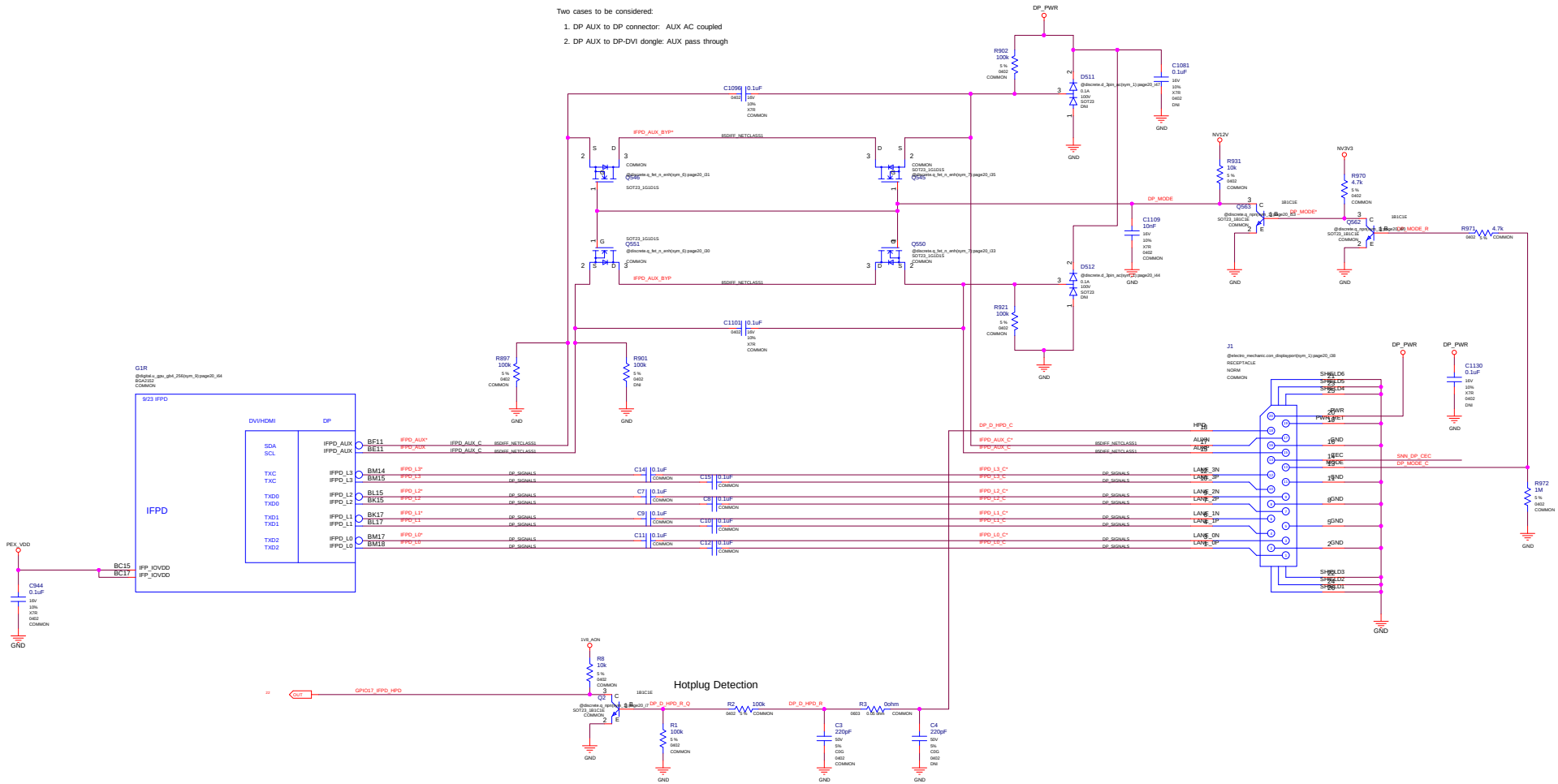
Page20: IFPD DP



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PAGE DETAIL	IFPD DP

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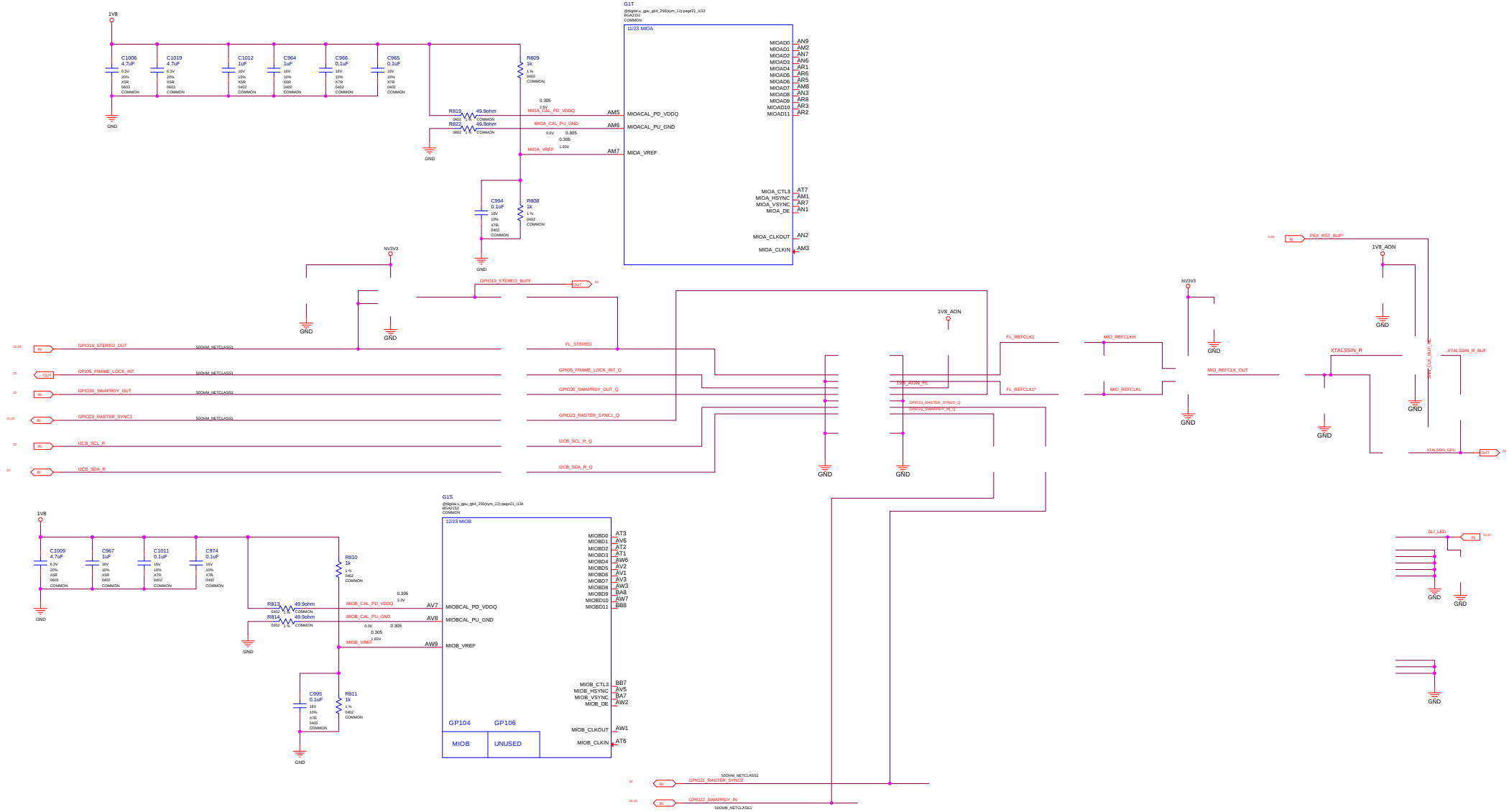
Page21: MIOA/B Interface and FRAME LOCK



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MIOA/B Interface and Frame Lock

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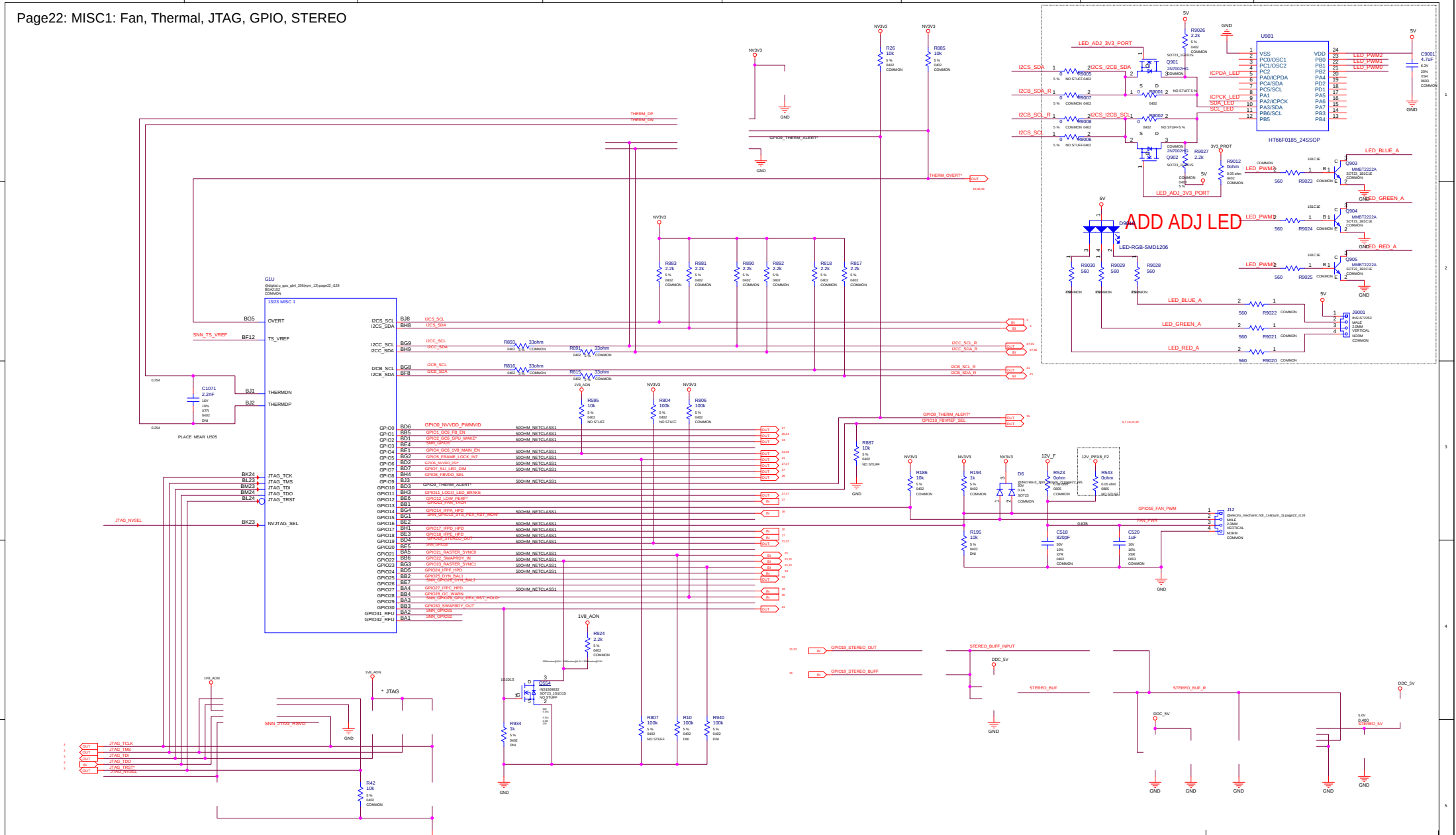
Page22: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

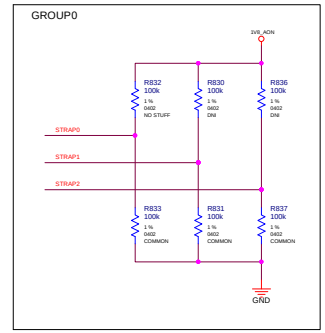
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

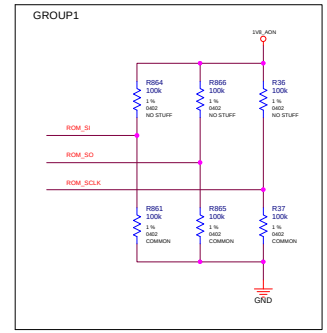
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

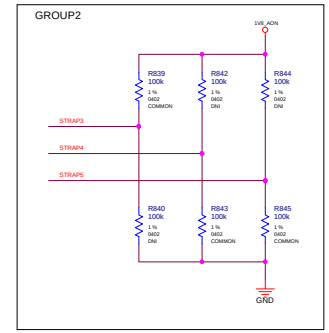
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

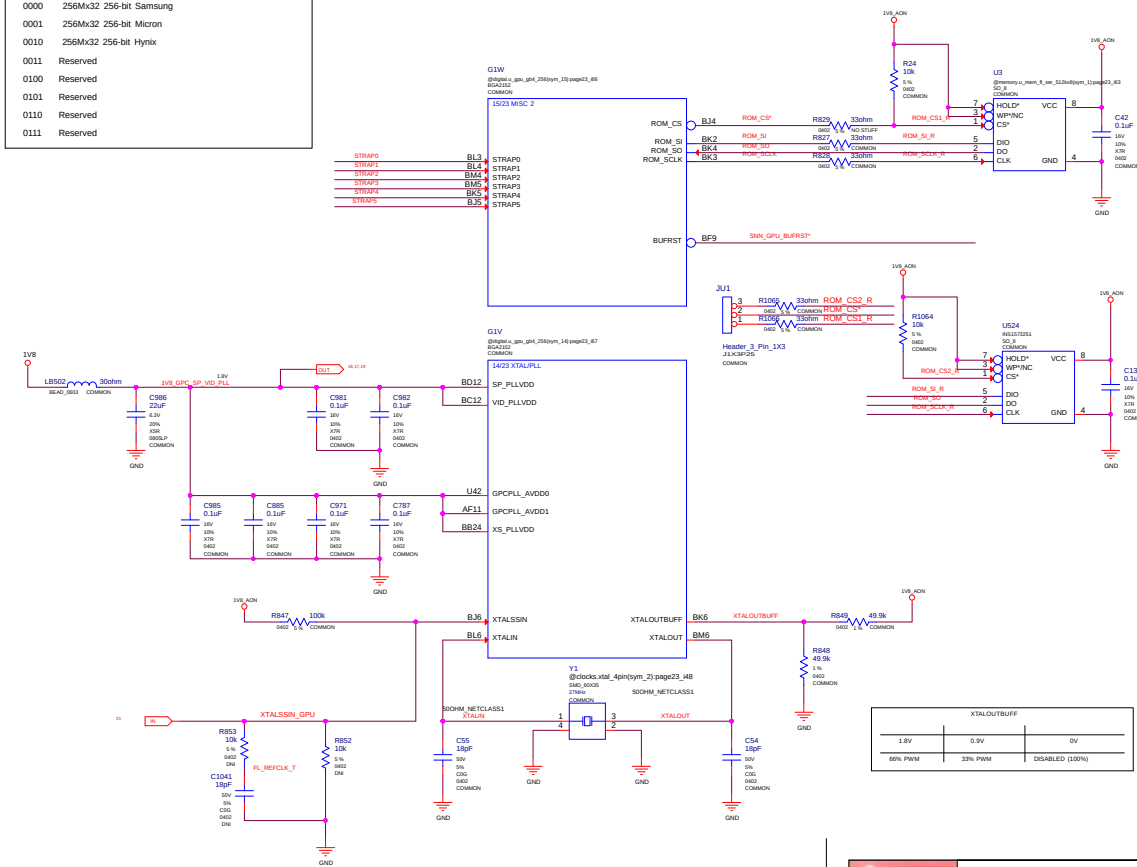
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







CFG[3:0]	Config	Width	Vendor
0000	256Mx32	256-bit	Samsung
0001	256Mx32	256-bit	Micron
0010	256Mx32	256-bit	Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL, Straps

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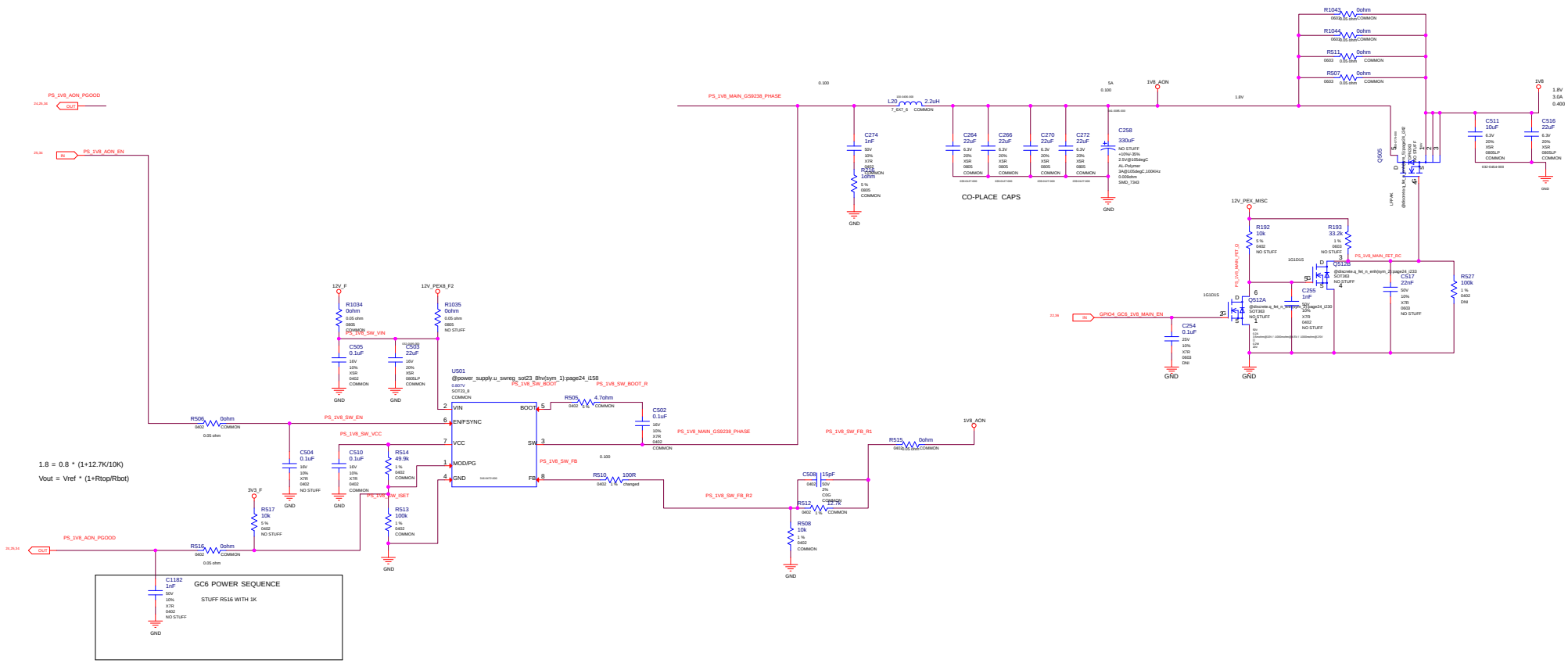
Page24: PS: 1V8, 1V8_AON



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PAGE DETAIL PS: 1V8, 1V8_AON

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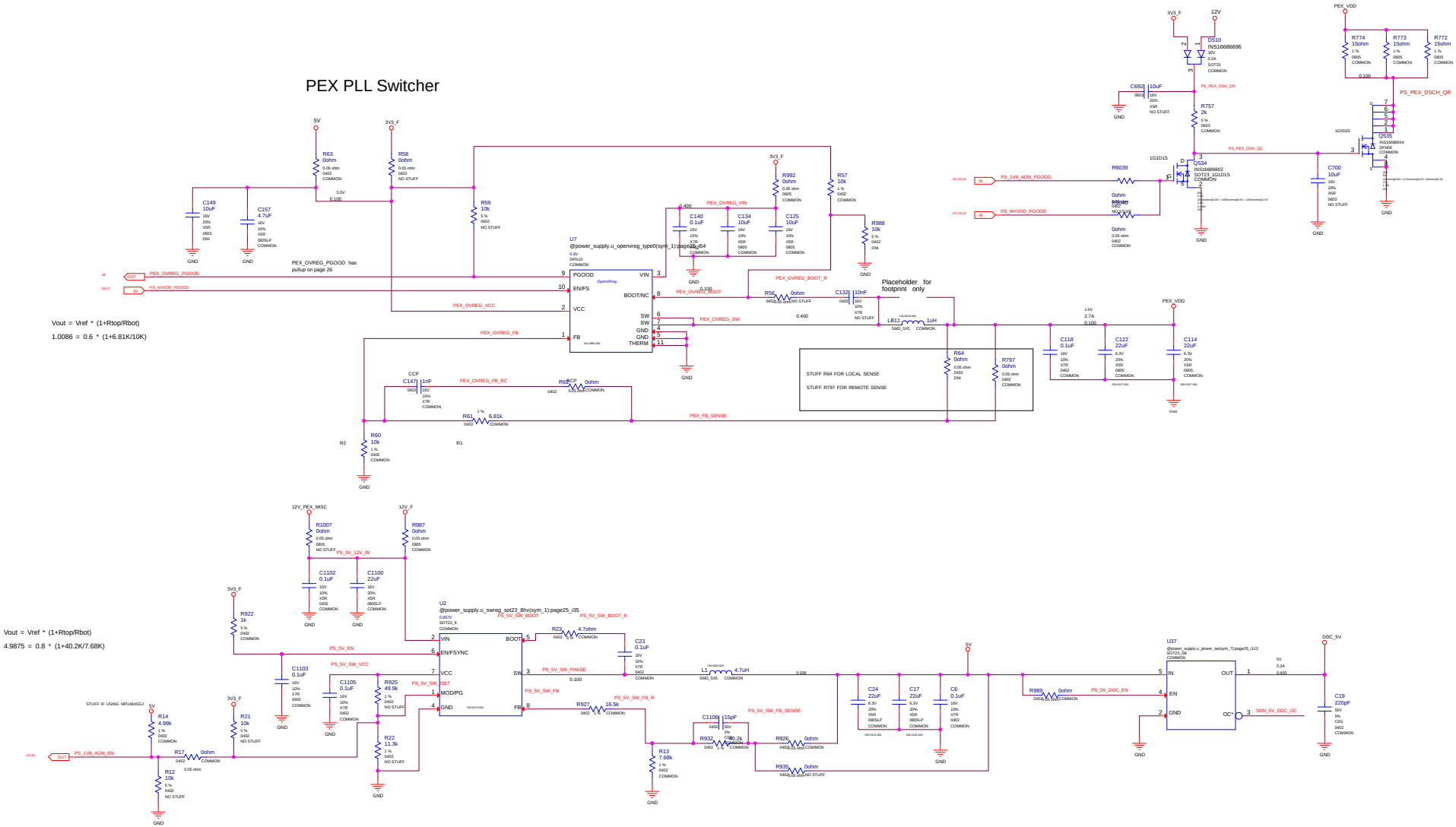
Page25: PS: 5V, PEX_VDD

PEX PLL Switcher


Vout = Vref * (1+Rtop/Rbot)
1.0086 = 0.6 * (1+6.81K/10K)
PEX_OVREG_PGOOD has pullup on page 26
Placeholder for footprint only
STUFF R64 FOR LOCAL SENSE
STUFF R797 FOR REMOTE SENSE
Vout = Vref * (1+Rtop/Rbot)
4.9875 = 0.8 * (1+40.2K/7.68K)
STUFF IF USING MP1484SGJ

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 5V, PEX_VDD

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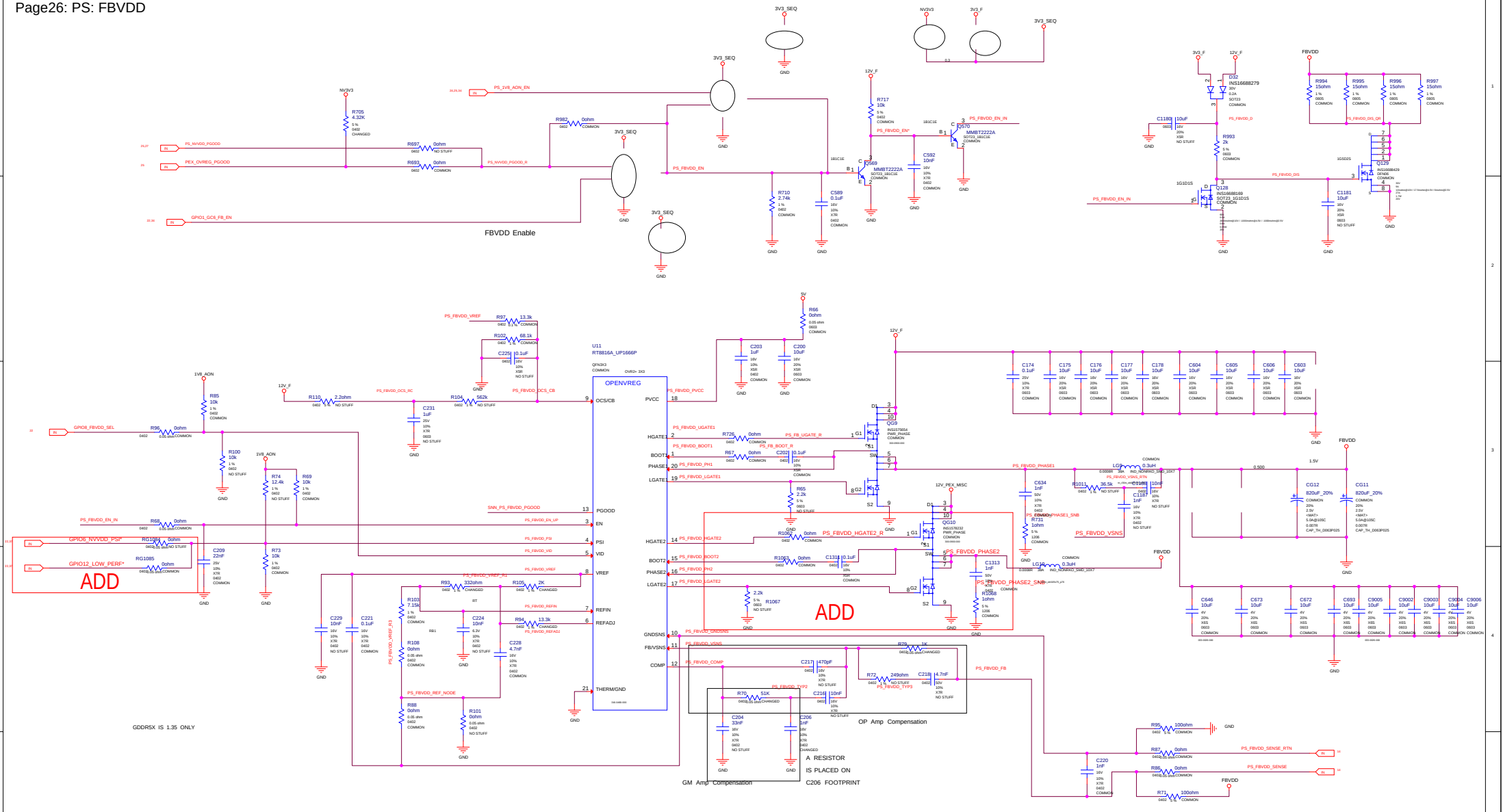
Page26: PS: FBVDD



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PAGE DETAIL	PS: FBVDD

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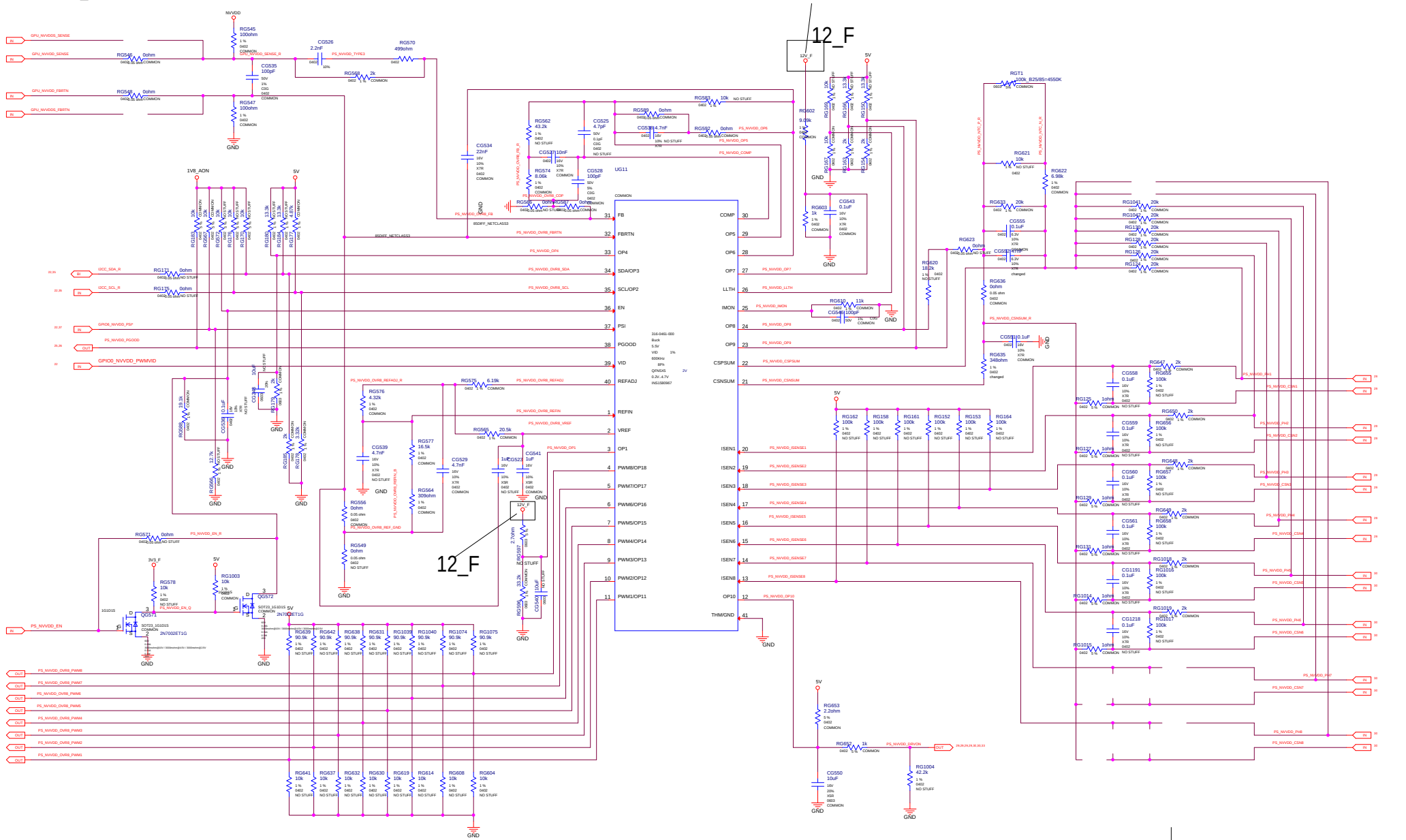
Page27: PS: NVVDD_OVR8



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
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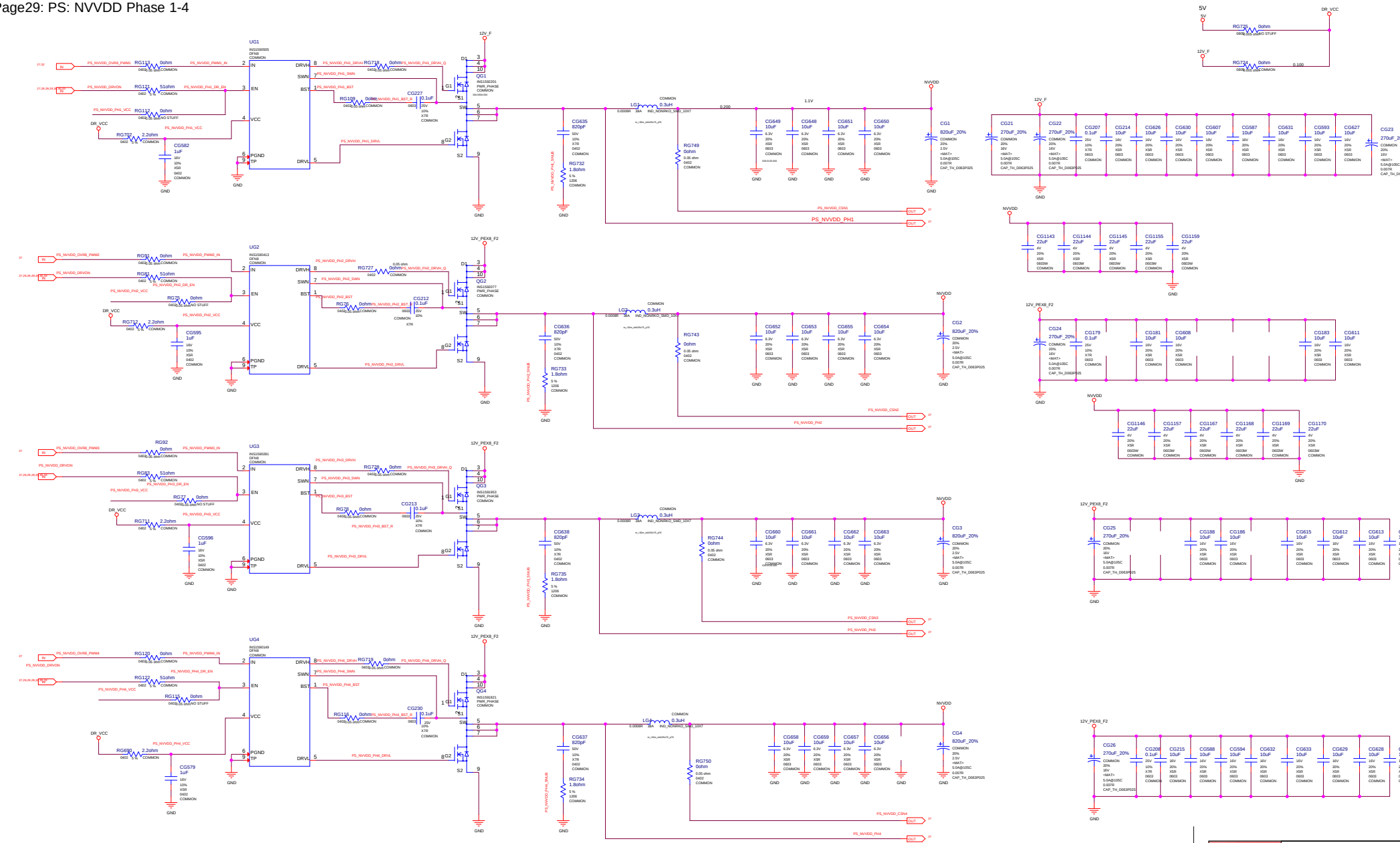
Page29: PS: NVVDD Phase 1-4



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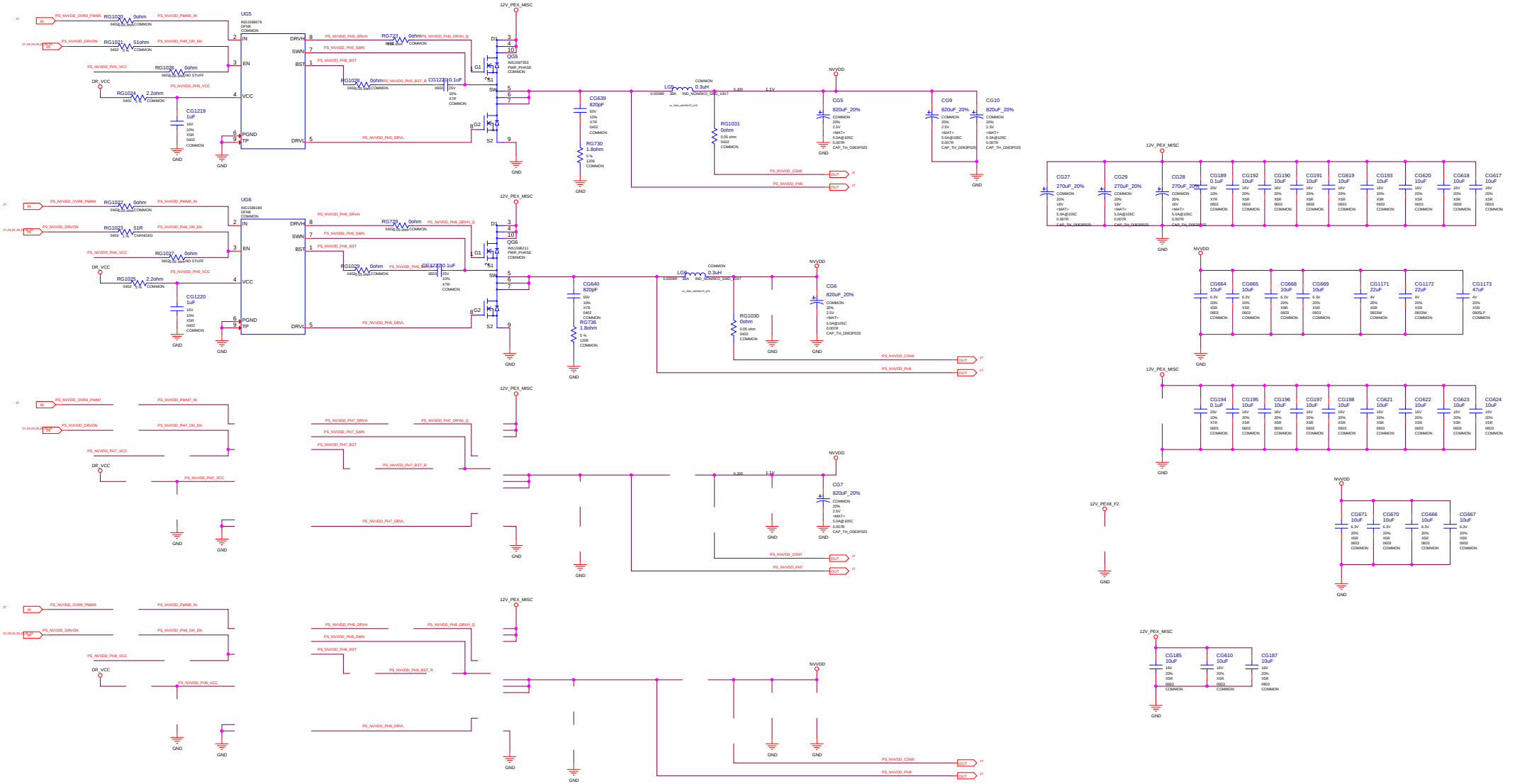
Page30: PS: NVVDD Phase 5 & 6



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 5 & 6

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Blank Page

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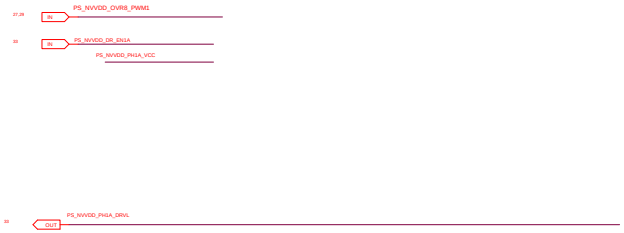
Page32: PS: Dynamic Power Balance Phases



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Dynamic Power Balance Phases

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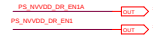
Page33: PS: Dynamic Power Balance Logic



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Dynamic Power Balance Logic

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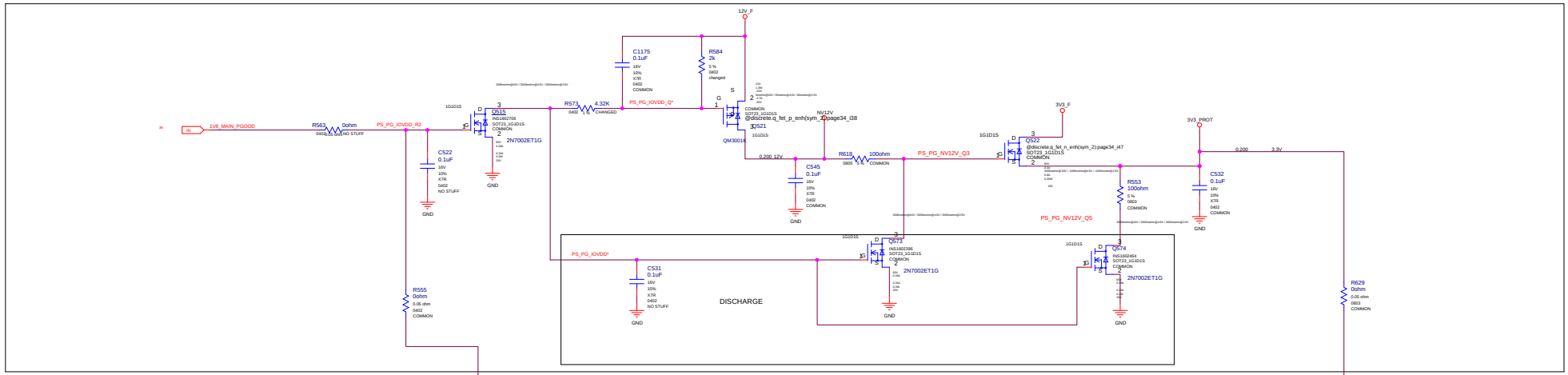
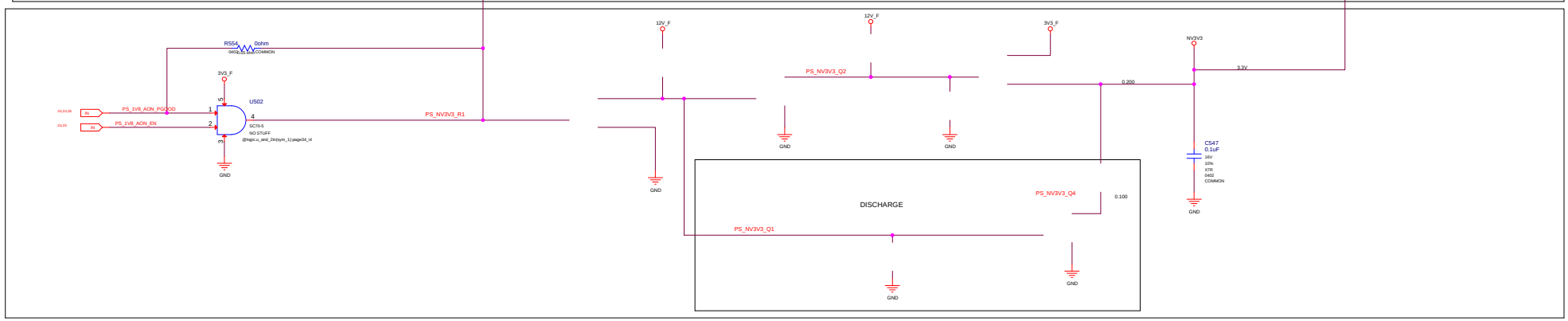
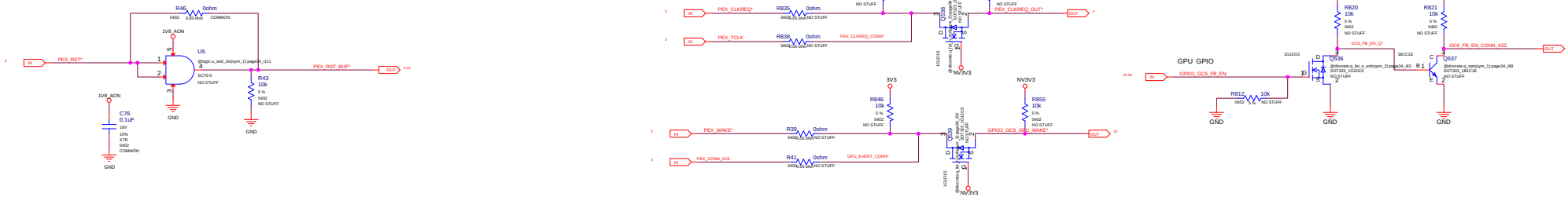
Page34:PS: NV3V3, NV12V







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NV3V3, NV12V

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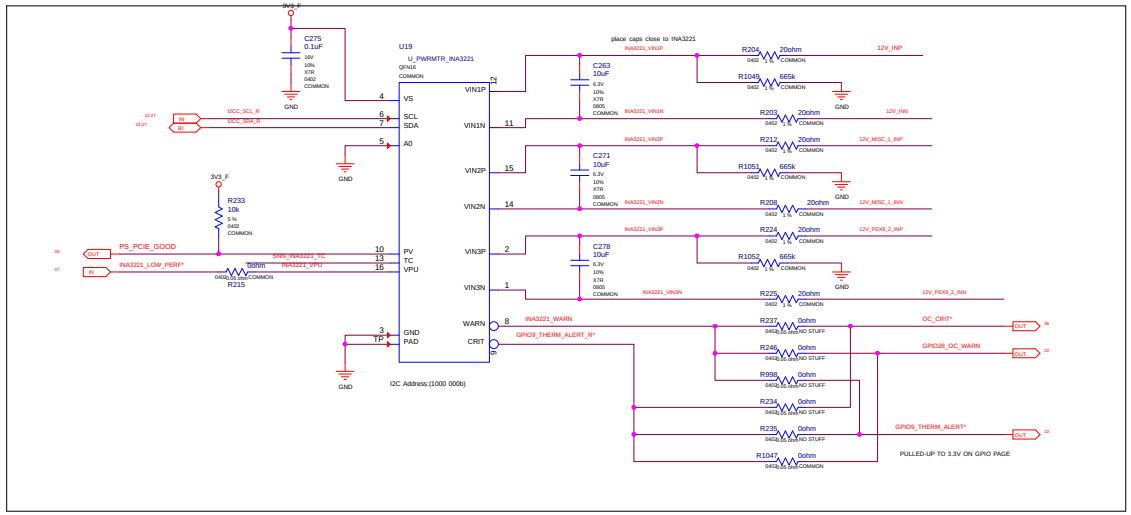
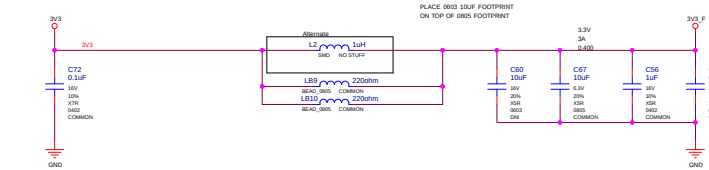
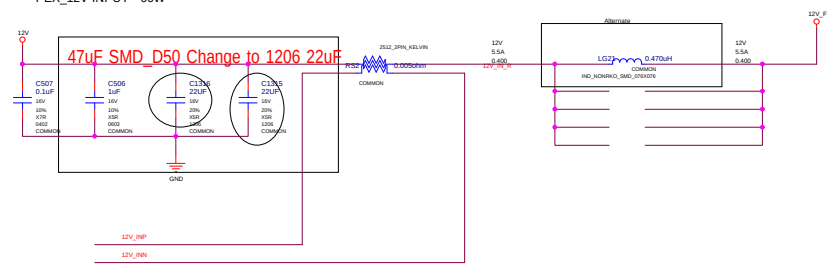
Page35: PS: Inputs, Filtering, and Monitoring

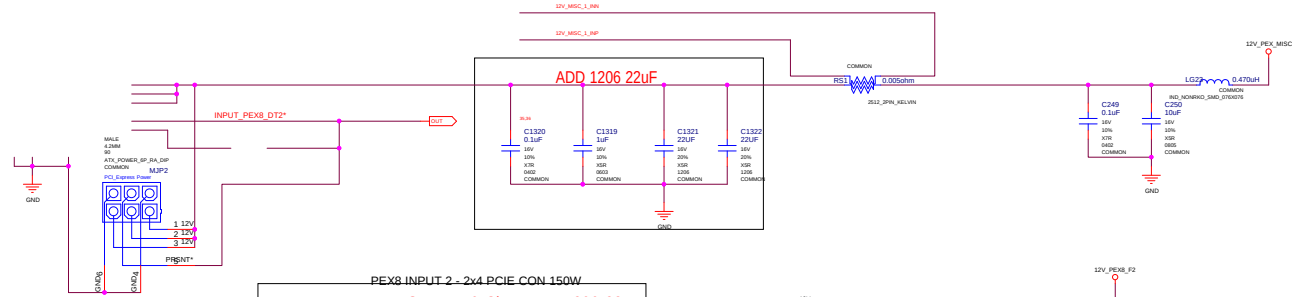


PEX 3V3 INPUT - 10W

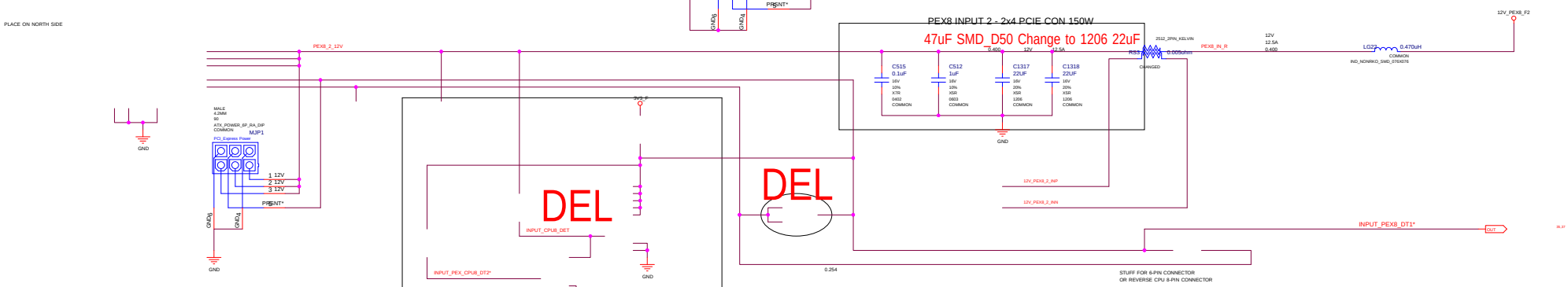


PEX_12V INPUT - 66W





PEX8 INPUT 2 - 2x4 PCIE CON 150W



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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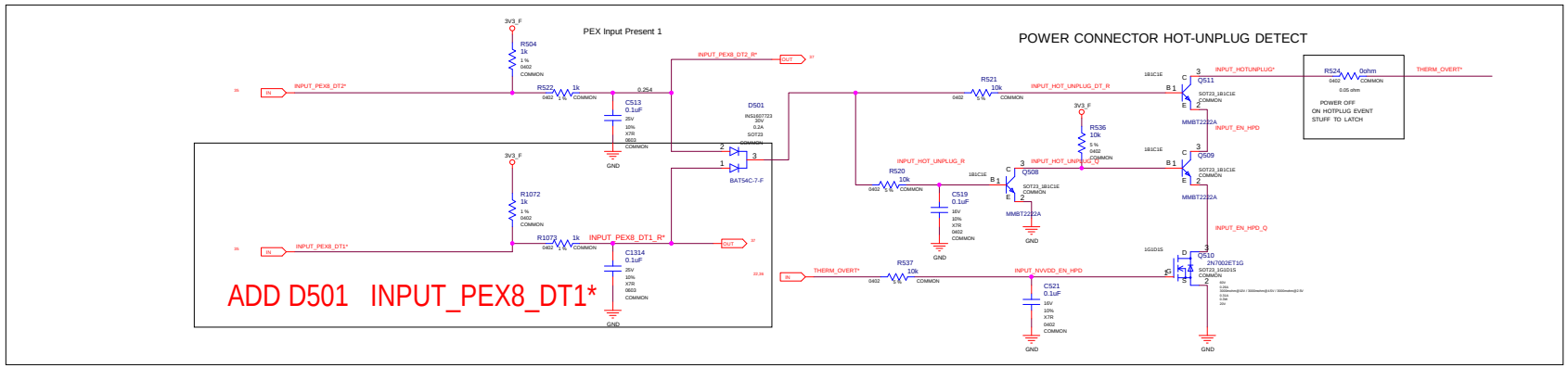

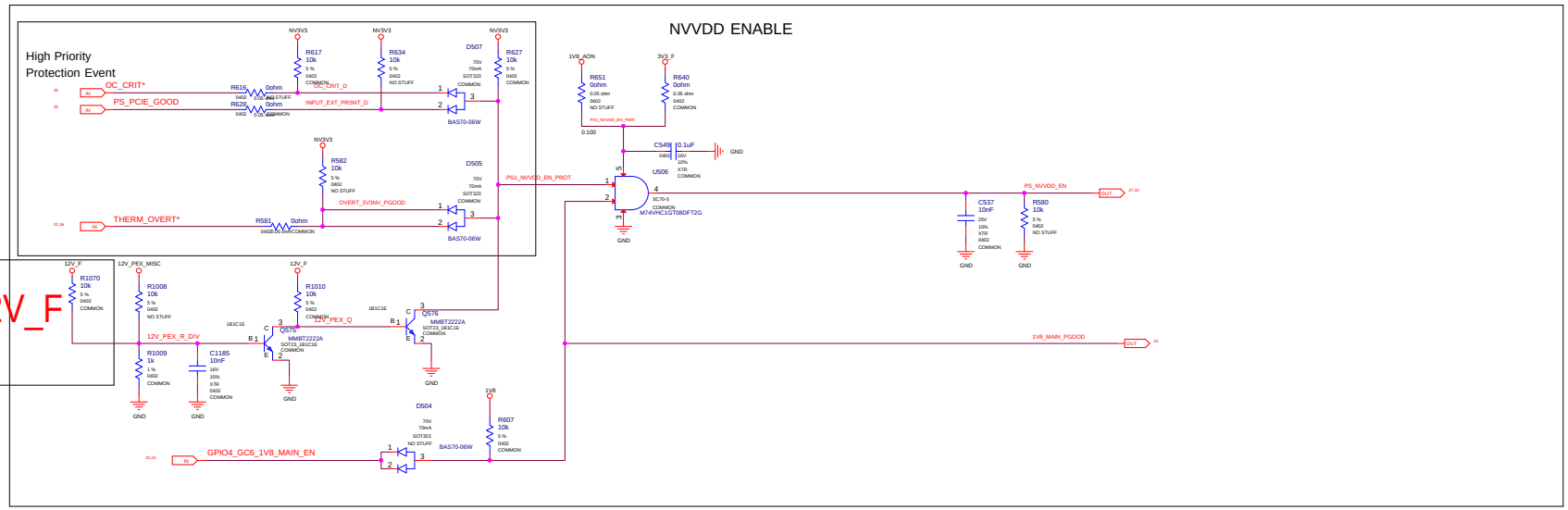

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Shutdown and Sequencing

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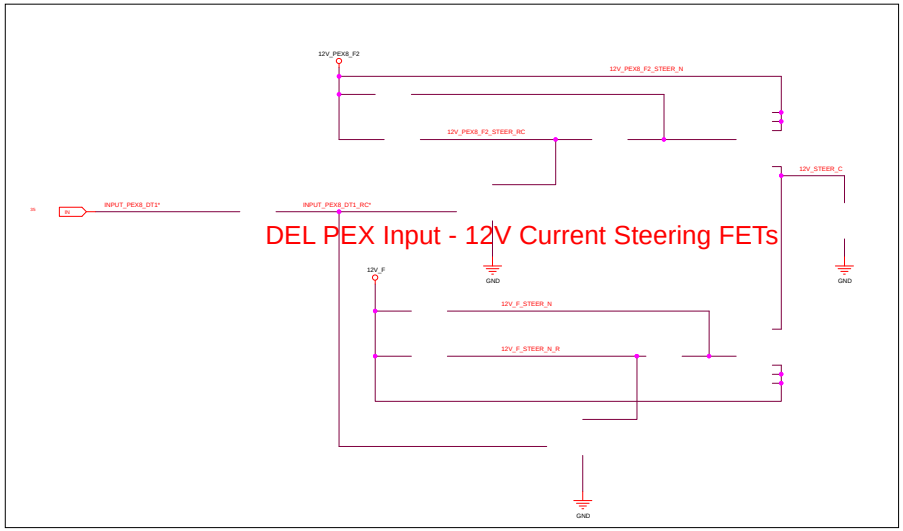
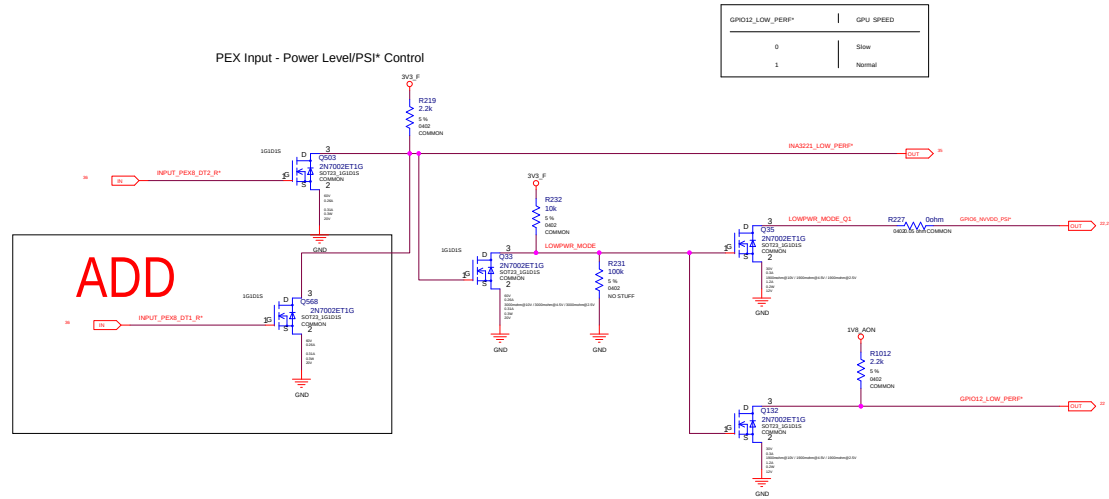
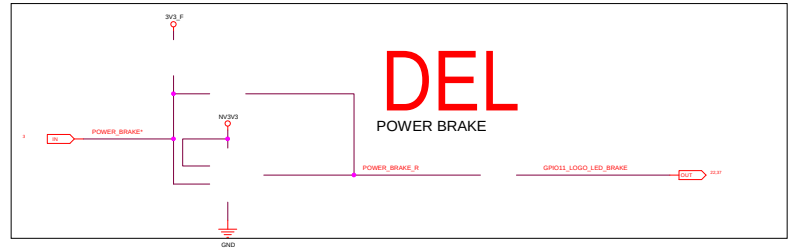
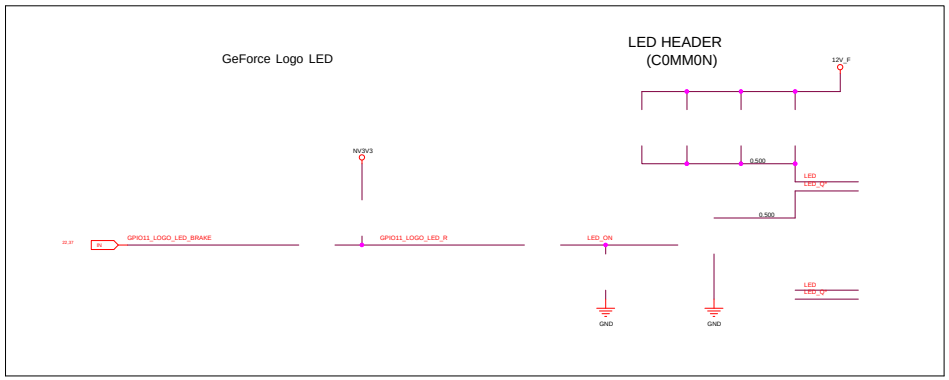
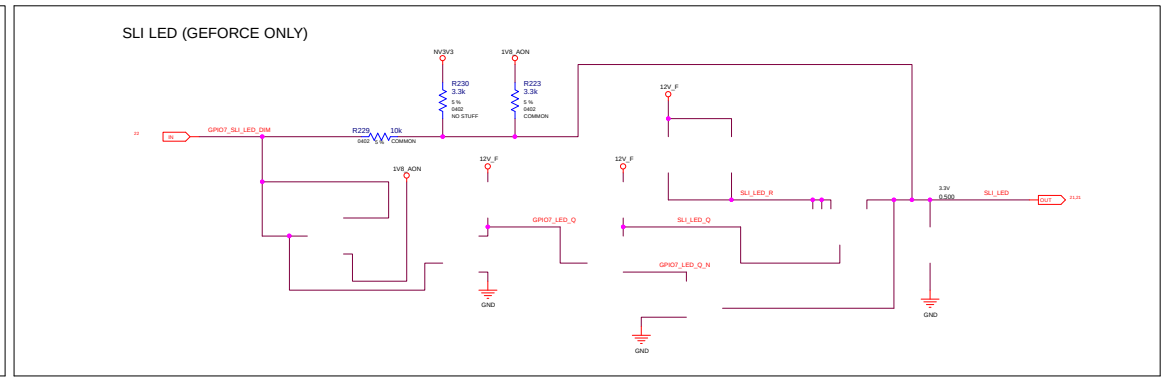
Page37: PS: 12V Current Steering, PSI Control, and LED











ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 12V Current Steering PSI Control and LED

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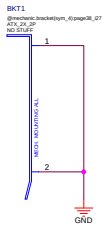
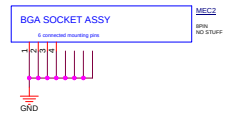
Page38: Mechanical: Bracket/Thermal Solution

Brackets:



GPU Stiffner



Mechanical Holes Symbol

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH: Bracket/Thermal

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